TOSHIBA Mobile IO Controller

TC6391XB

Tentative Specification

Rev. 0.90a 2002-02-25

TOSHIBA CORPORATION

Revision History

TITLE: TC6391XB Tentative Specification

REV NO.	DATE	CONTENTS	REVISED by	APP'D by
0.90a	2002-02-25	Released 1st edition	S. Ueta	T. Takada

Contents

1. Overview

TOSHIBA develops a companion chip, called TC6391XB, which can be connected to the Strong ARM(SA1110/XScale) made by Intel corporation. This chip is equipped with Standard Memory interface with 16-bit bus. TC6391XB is a controller LSI for SD memory card, SDIO card, SmartMedia and USB devices. In addition, TC6391XB holds Serial I/O controller for PDC/cdmaOne and some logic for controlling PCMCIA(CompactFlash) card and low Polysilicon TFT. This companion chip enables not only complete system to be built with greatly reduced chip count, but also low power consumption which is performed by using both buffer off function with #SUSPEND and gated clock control.

1.1 Chip Specifications

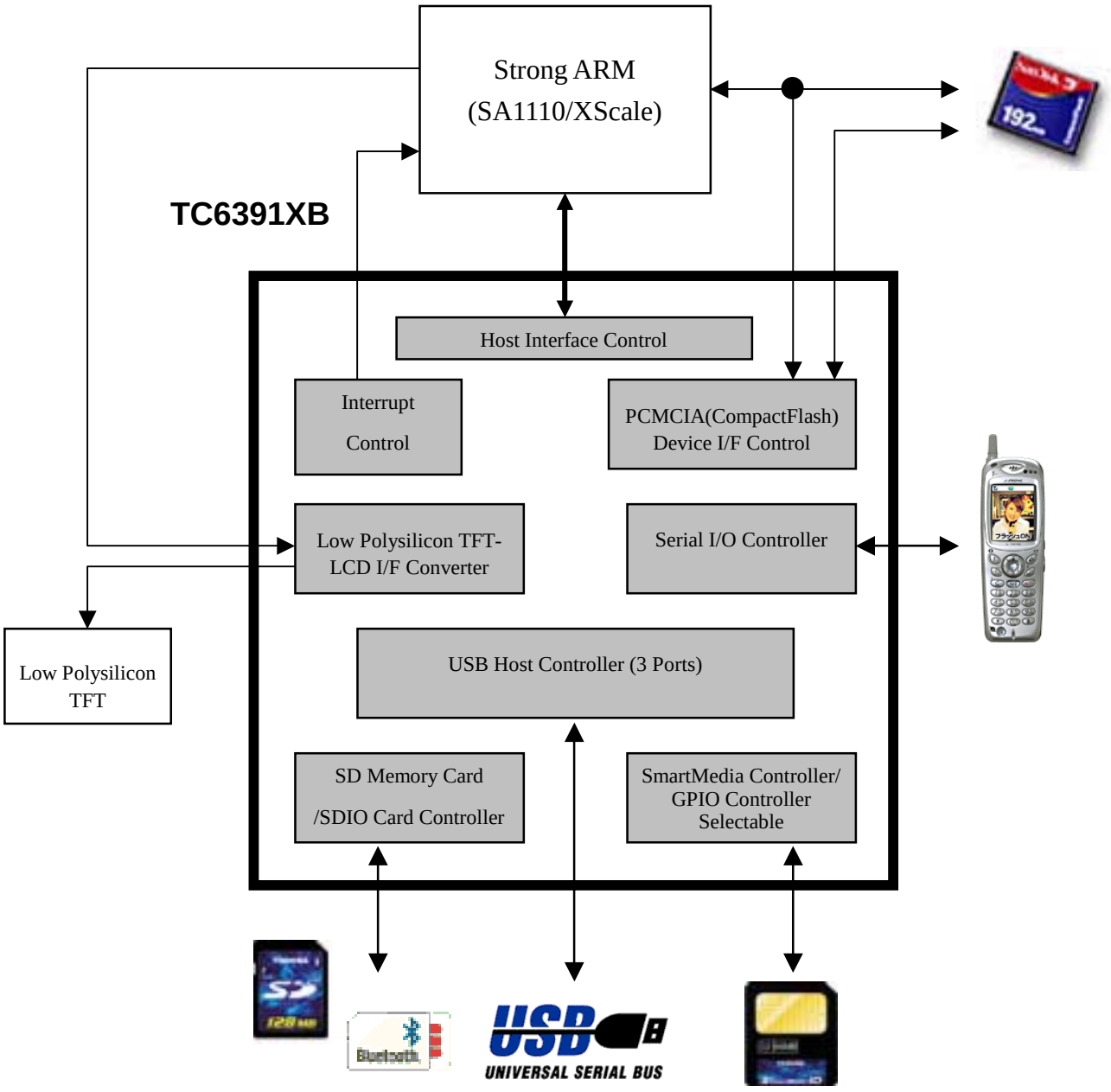
- 0.35um CMOS Process
- 0.8mm Ball Pitch 225-pin PBGA Package

View of TC6391XB

1.2 Specification Overview

- Standard Memory Interface
- Supports interrupt
- Clock Frequency : Max.33MHz
- Supports SD Card 1 Slot
- Conforms to SD Memory Card Physical Layer Specification Version 1.0
  - Operating frequency Max.25MHz
  - Offers MultiMedia Card write/read
  - Offers multi-block write/read
  - Does not support SPI mode
  - Supports double buffers(512byte*2)
- Conforms to SDIO Card Specification Version 1.0
  - Operating frequency Max.25MHz
  - Offers multi-block write/read
  - Does not support SPI mode
  - Supports 64byte buffer
- Conforms to SmartMedia Electric Specification Version 1.2 and SmartMedia Physical Format Specification Version 1.2
  - Supports 3.3V SmartMedia (Does not support 5.0V media)
  - Supports hardware ECC
  - SmartMedia interface signals can be assigned to GPIO interfaces
- Conforms to Universal Serial Bus Specification Version 1.1
  - Supports 3 ports
- Supports Serial I/O Controller(for PDC/cdmaOne)
  - Supports Asynchronous Receiver/Transmitter 2 ports
  - Supports Synchronous Receiver/Transmitter 1 port
- Supports Low Polysilicon TFT-LCD Interface converter
  - Includes any logic for controlling Low Polysilicon TFT
- PCMCIA(CompactFlash) Device I/F Control
  - Includes any logic for controlling PCMCIA(CompactFlash)

2. Block Diagram



3. Signals

3.1 Pin Assignments

Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	VSS	USB2DN	USB3DP	CPH	STH	XCK	NXCK	XST	NXST	YCK	RRXD	VSS	#RDSR	RTXD	VSS	1
2	USB1DN	NC	NC	USB3DN	NYCK	YST	NYST	COM	PREC	#PREC	#RCTS	#RDCD	#RRI	#RRTS	TXD0	2
3	#USBOC	USB1DP	USB2DP	NC	PPOL	#PPOL	LHSYNC	LVSYNC	LDE	LSCLK	#S2CD1	#S2CD2	SMCLE	#RDTR	RXD0	3
4	VSS	PPON1	PPON2	NC	NC	TST0	TST1	TST2	TST3	#P2CD	#S2DOE	#S2WAIT	SMALE	SMD7	FRM0	4
5	SDCD3	SDCMD	SDLED	PPON3	NC	VDD	VDD	NC	VDD	VDD	#S2COE	#S2IOIS16	#SMWE	SMD6	SCK0	5
6	SDCD2	SDCLK	SDPWR	#DIR	VDD	VSS	VSS	VSS	VSS	VSS	VDD	#SMLED	#SMRE	SMD5	TXD1	6
7	SDCD1	SDWP	#SDCD	#S1IOIS16	VDD	VSS	VSS	VSS	VSS	VSS	VDD	#SMLOCK	#SMCE	SMD4	#RTS1	7
8	SDCD0	RSV1	SRSEL	#S1WAIT	VDD	VSS	VSS	VSS	VSS	VSS	VDD	#SMEJCT	#SMWP	SMD3	RXD1	8
9	#SUSPEND	DISEL1	LVSEL	#S1CD2	VDD	VSS	VSS	VSS	VSS	VSS	VDD	SMVC3EN	SMD1	SMD2	#CTS1	9
10	#PCLR	CLK32	DMDAT	#S1CD1	VDD	VSS	VSS	VSS	VSS	VSS	VDD	#SMRB	SMD0	#CONT2	RVON	10
11	DISEL0	RSV0	L3VON	#S1DOE	HRDY	VDDS	VDDS	VDD	VDDS	VDDS	VDDS	#SMCD	#SMWPD	#DTR1	#CONT1	11
12	CK48M	HCLK	#S1COE	#PIO16	PSKTSEL	#HOE	HA10	HA6	HA2	VSS	HD10	SMLVD	#SMEJSW	#PUPD	VSS	12
13	#RSV0	RSV2	#P1CD	#PWAIT	#HBEH	#HCS	HA9	HA5	HA1	HD13	HD9	HD6	HD3	#DET1	#DSR1	13
14	#HINT	#PIOR	#PCE2	HA13	#HBEL	HA12	HA8	HA4	HD15	HD12	HD8	HD5	HD2	SEL1	SEL0	14
15	VSS	#POE	#PCE1	VSS	#HWE	HA11	HA7	HA3	HD14	HD11	HD7	HD4	HD1	HD0	VSS	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

3.2 Pin Signals

Host Interface (35-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
HD15	J14	IO *1	VDDS	System Data 15-0
HD14	J15			
HD13	K13			
HD12	K14			
HD11	K15			
HD10	L12			
HD9	L13			
HD8	L14			
HD7	L15			
HD6	M13			
HD5	M14			
HD4	M15			
HD3	N13			
HD2	N14			
HD1	N15			
HD0	P15			
HA13	D14	I	VDDS	System Address 13-1
HA12	F14	I		
HA11	F15	I		
HA10	G12	I		
HA9	G13	I		
HA8	G14	I		
HA7	G15	I		
HA6	H12	I		
HA5	H13	I		
HA4	H14	I		
HA3	H15	I		
HA2	J12	I		
HA1	J13	I		
#HCS	F13	I		Chip Selection
#HOE	F12	I		Output Enabled
#HWE	E15	I		Write Enabled
#HBEL	E14	I		Byte Enabled L
#HBEH	E13	I		Byte Enabled H
HRDY	E11	O (OD) *2	VDD	Ready

*1 Buffer with pull-down resistance
*2 Levels cannot be converted.

Pin Signals (cont'd)

SD Card Interface (9-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
SDCD3	A5	IO	VDD	SD Card Slot /Data Bus
SDCD2	A6			
SDCD1	A7			
SDCD0	A8			
SDCMD	B5	IO		SD Card Slot /Command
SDCLK	B6	O		SD Card Slot / Clock
#SDCD	C7	I *		SD Card Slot /Detection
SDWP	B7	I *		SD Card Slot /Write Protection Media is write-protected when this Pin indicates "High".
SDLED	C5	O		SD Card Slot /signal for LED

* Buffer with pull-up resistance

SD Card Power Supply Control (1-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
SDPWR	C6	O	VDD	SD Card Slot/ Power Supply Control. 3.3V Enable Signal

Pin Signals (cont'd)

SmartMedia™ Interface (22-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
SMD7/GPI7	P4	IO *1	VDD	Data
SMD6/GPI6	P5			
SMD5/GPI5	P6			
SMD4/GPI4	P7			
SMD3/GPI3	P8			
SMD2/GPI2	P9			
SMD1/GPI1	N9			
SMD0/GPI0	N10			
SMCLE/GPO5	N3	O (3state)		Command Latch Enabled
SMALE/GPO4	N4	O (3state)		Address Latch Enabled
#SMWE/GPO3	N5	O (3state)		Write Enabled
#SMRE/GPO2	N6	O (3state)		Read Enabled
#SMCE/GPO1	N7	O (3state)		Chip Enabled
#SMWP/GPO0	N8	O (3state)		Write Protection
#SMRB/GPI12	M10	I		Busy
#SMCD/GPI11	M11	I *2		Card Detection
SMLVD/GPI10	M12	I *2		Low-Voltage Detection
#SMWPD/GPI9	N11	I *2		Write Protection Seal Indicates Write-Protected Media being inserted when this Pin indicates "Low".
#SMEJSW/GPI8	N12	I *2		Ejects request. When H, a media is inserted. When L, no media is inserted. Changes detection control to one where L indicates a media is inserted by setting bit 7 of the SmartMedia™ host controller's configuration register 63h.
#SMLED	M6	O (OD) *3		LED ON
#SMLOCK	M7	O (OD) *3		Lock Mode
#SMEJCT	M8	O (OD) *3		Ejection Response

*1 Buffer with pull-down resistance.
*2 Buffer with pull-up resistance.
*3 Levels cannot be converted.

SmartMedia™ Power Supply Control (1-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
SMVC3EN/GPO6	M9	O	VDD	Power Supply Control. VDD3.3V Enable Signal

Pin Signals (cont'd)

USB Host Interface (10-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
USB1DP	B3	IO	VDD	USB Port 1 Data+
USB1DN	A2			USB Port 1 Data-
USB2DP	C3			USB Port 2 Data+
USB2DN	B1			USB Port 2 Data-
USB3DP	C1			USB Port 3 Data+
USB3DN	D2			USB Port 3 Data-
PPON1	B4	O		USB Port 1/Power Supply Control
PPON2	C4	O		USB Port 2/Power Supply Control
PPON3	D5	O		USB Port 3/Power Supply Control
#USBOC	A3	I		USB Over Current

Pin Signals (cont'd)

Serial Port Interface (25-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
TXD0	R2	O	VDD	Synchronous Send Data
RXD0	R3	I		Synchronous Receive Data
FRM0	R4	I		Frame Clock
SCK0	R5	I		Serial Clock
TXD1	R6	O		Asynchronous Send Data
#RTS1	R7	O		Request to Send
RXD1	R8	I		Asynchronous Receive Data
#CTS1	R9	I		Clear to Send
RRXD	L1	O		Asynchronous Receive Data to Host
#RCTS	L2	O		Clear to Send to Host
#RDCD	M2	O		Data Carrier Detect to Host
#RDSR	N1	O		Data Set Ready to Host
#RRI	N2	O		Ring Indicate to Host
RVON	R10	O		Power Switch select to Driver/Receiver
RTXD	P1	I		Asynchronous Send Data from Host
#RRTS	P2	I		Request to Send from Host
#RDTR	P3	I		Data Terminal Ready from Host
#CONT2	P10	O		Serial Port control
#CONT1	R11	O		Serial Port control
#DTR1	P11	O		Data Terminal Ready to
#PUPD	P12	O		Pull-up/Pull-down control
#DSR1	R13	I		Data set Ready from
#DET1	P13	I		Device detect
SEL1	P14	I *		External Device select
SEL0	R14	I *		External Device select

* Buffer with pull-up resistance

Pin Signals (cont'd)

CompactFlash Control Interface (22-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
#P1CD	C13	O	VDD	Slot1 detect to SA
#P2CD	K4	O		Slot2 detect to SA
#PWAIT	D13	O	VDDS	Wait to SA
#PIO16	D12	O		16bit I/O access to SA
#S1COE	C12	O	VDD	Slot1 control signal output enable
#S2COE	L5	O		Slot2 control signal output enable
#DIR	D6	O		Data direction control(1:Write / 0:Read)
#S1DOE	D11	O		Slot1 data output enable
#S2DOE	L4	O		Slot2 data output enable
#S1CD2	D9	I *		Slot1 detect from Card
#S1CD1	D10	I *		Slot1 detect from Card
#S2CD2	M3	I *		Slot2 detect from Card
#S2CD1	L3	I *		Slot2 detect from Card
#S1WAIT	D8	I *		Slot1 Wait from Slot
#S2WAIT	M4	I *		Slot2 Wait from Slot
#S1IOIS16	D7	I *		Slot1 16bit I/O access from Card
#S2IOIS16	M5	I *		Slot2 16bit I/O access from Card
#PCE2	C14	I	VDDS	Card enable from SA
#PCE1	C15	I		Card enable from SA
#POE	B15	I		Output enable from SA
#PIOR	B14	I		I/O read from SA
PSKTSEL	E12	I		Slot select(1:Slot2 / 0:Slot1)

* Buffer with pull-up resistance

Pin Signals (cont'd)

Low Polysilicon TFT-LCD Converter Control Interface (19-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
CPH	D1	O	VDD	Clock to DAC
STH	E1	O		DAC sampling start to DAC
XCK	F1	O		X clock to LCD
NXCK	G1	O		X clock (Negative) to LCD
XST	H1	O		X shift register start to LCD
NXST	J1	O		X shift register start (Negative) to LCD
YCK	K1	O		Y clock to LCD
NYCK	E2	O		Y clock (Negative) to LCD
YST	F2	O		Y shift register start to DAC/LCD
NYST	G2	O		Y shift register start (Negative) to LCD
COM	H2	O		Common control to LCD
PREC	J2	O		Pre-charge to LCD
#PREC	K2	O		Pre-charge (Negative) to LCD
PPOL	E3	O		Polarity reverse to DAC
#PPOL	F3	O		Polarity reverse (Negative) to DAC
LHSYNC	G3	I		Flat Panel Horizontal sync from LCDC
LVSYNC	H3	I		Flat Panel Vertical sync from LCDC
LDE	J3	I		Flat Panel Data enable from LCDC
LSCLK	K3	I		Flat Panel Shift clock from LCDC

Pin Signals (cont'd)

SYSTEM Interface (12-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
HCLK	B12	I	VDD	System Clock (max.33MHz)
CK48M	A12	I		External Clock(max.48MHz)
CLK32	B10	I		Used for a SD card detection.
#HINT	A14	O(OD)*1		Interruption
#PCLR	A10	I		All registers are cleared when this signal is asserted
#SUSPEND	A9	I		Suspend
DISEL1	B9	I		Device I/F Selection 1-0 *2
DISEL0	A11	I		
SRSEL	C8	I		Switch On/Off for internal pull-down resister. This signal can control internal pull-down resister of HD[15:0]. 1 : Internal pull-down resister Off 0 : Internal pull-down resister On
LVSEL	C9	I		Switch voltage of VDDS 1 : VDDS=3.3V 0 : VDDS=2.5V
DMDAT	C10	O		LCD panel dummy data
L3VON	C11	I		LCD 3.3V on

*1 Levels cannot be converted.

*2 SmartMedia interface signals can be used as GPIO interface signals by setting DISEL[1:0] signals. Do not apply dynamic switching for certain items in DISEL 1-0 (Items that switches interface and are uniquely configured for the system).

DISEL1-0	SmartMedia I/F signals
00	SmartMedia I/F
01	SmartMedia I/F
10	GPIO I/F
11	Reserved

Pin Signals (cont'd)

TEST Pin (4-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
TST0	F4	I	VDD	Test Mode Signal 3,2,1,0 Utilized for Test Mode Set "0000" for TST[3-0] under normal circumstances.
TST1	G4			
TST2	H4			
TST3	J4			

Other Pins (4-pin)

NAME	Pin	IO	Power Supply	FUNCTION/REMARKS
#RSV0	A13	O(OD)	3.3	Open
RSV0	B11	I		Fixed to direct GND.
RSV1	B8	I		Fixed to direct GND.
RSV2	B13	I		Fixed to direct GND.

3.3 Power Supply/GND (54 pins)

NAME	Pin	FUNCTION/REMARKS
VSS	A1, M1, R1, A4, F6, G6, H6, J6, K6, F7, G7, H7, J7, K7, F8, G8, H8, J8, K8, F9, G9, H9, J9, K9, F10, G10, H10, J10, K10, K12, R12, A15, D15, R15	GND(34 pins)
VDD	F5, G5, J5, K5, E6, L6, E7, L7, E8, L8, E9, L9, E10, L10, H11	3.3V(15 pins)
VDDS	F11, G11, J11, K11, L11	2.5V/3.3V(5 pins)

3.4 Summary: Interface Pins

Interface		# of Pins	Remarks
Host		35	
SD Card		9	
SD Card Power Supply Control		1	
SmartMedia™		22	
SmartMedia™ Power Supply Control		1	
USB Host		10	
Serial Port		25	
Compact Flash Control		22	
Low Polysilicon TFT-LCD Converter Control		19	
System		12	
TEST		4	
Other		4	
	Total	164	
GND		34	
VDD		15	
VDDS		5	
NC		7	Open
	Grand Total	225	

4. Functionality Descriptions

4.1 Host Interface

TC6391XB supports standard memory interfaces and the following suggests examples of circuits for connecting to Standard Memory Interface:

Standard Memory	TC6391XB
A13-1	HA13-1
D15-0	HD15-0
-CS	#HCS
-OE	#HOE
-WE	#HWE
-BEH	#HBEH
-BEL	#HBEL
-RDY	HRDY

4.2 Resource Area

TC6391XB holds the following Resource Area:

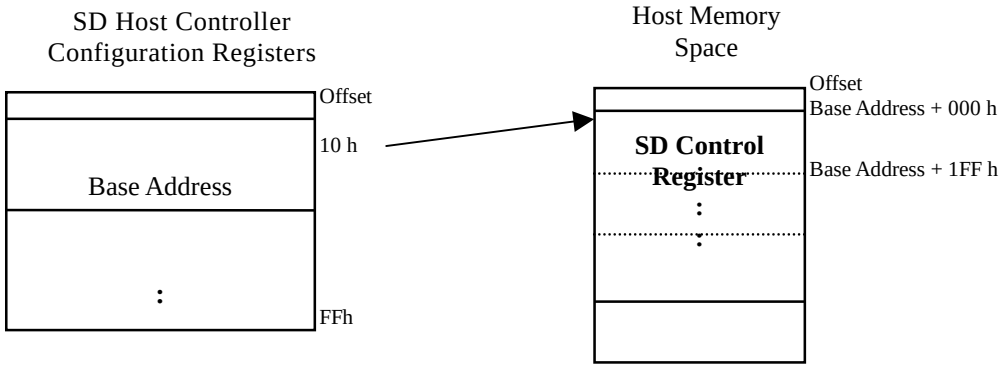
1) System Configuration Area
2) SmartMedia™ Host Controller Configuration Area
3) SmartMedia™ Control Register Area
4) SD Host Controller Configuration Area
5) SD Control Register Area
6) USB Host Controller Register Area
7) USB Control Register Area
8) LCD & Serial Port Host Controller Register Area
9) LCD & Serial Port Control Register Area
10) Local Memory Area

See below for mapping of Configuration Area, Control Register Area for respective devices (SD, SM, USB and LCD & Serial port). Further, Control Register Area for respective devices are mapped to any memory resources(800-FFFh) by setting BASE Address Register in Configuration Area for respective devices.

Offset		FUNCTION/REMARKS
A13-12	A11-1	
00	000 - 0FFh	System Configuration Area
	100 - 1FFh	SmartMedia™ Host Controller Configuration Area
	200 - 2FFh	SD Host Controller Configuration Area
	300 - 3FFh	USB Host Controller Register Area
	400 - 4FFh	LCD & Serial Port Host Controller Register Area
	500 - 7FFh	Reserved for Configuration Area
	800 - FFFh	Control Register for respective devices (BASE Address Register of Configuration Register for respective devices—configurable in Offset10h--)
01	000 - FFFh	Local Memory Area 1 (4KB)
10	000 - FFFh	Local Memory Area 2 (4KB)
11	000 - FFFh	Reserved

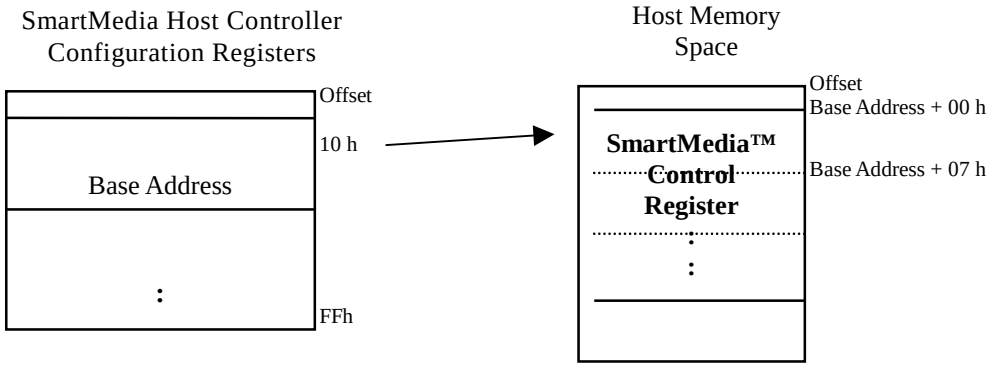
- SD Control Register Area

As for accessing Resource in SD Control Register Area, use Configuration Register Base Address Reg.(Config.offset: 10h) in SD Host Controller for mapping the settings to access designated Memory Areas (800-FFFh). However, SD Control Register Area cannot be mapped in IO Resource Area.



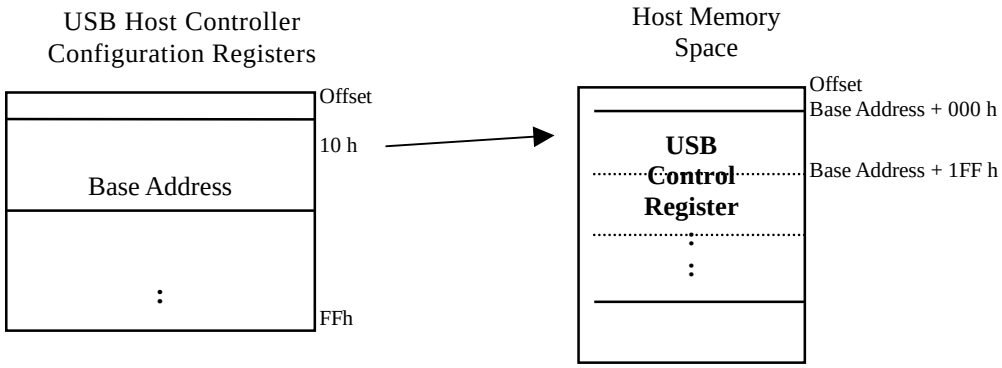
- SmartMedia™ Control Register Area

As for accessing SmartMedia™ Control Register Area, use Configuration Register Base Address Reg.(Config.offset: 10h) in SmartMedia™ Host Controller for mapping the settings to access designated Memory Areas (800-FFFh). However, SmartMedia™ Control Register Area cannot be mapped in IO Resource Area.



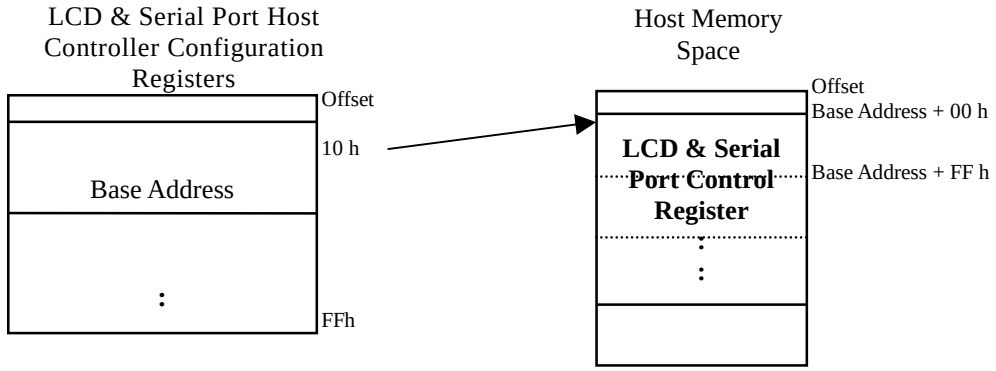
- USB Control Register Area

As for accessing USB Control Register Area, use Configuration Register Base Address Reg.(Config.offset: 10h) in USB Host Controller for mapping the settings to access designated Memory Areas (800-FFFh). However, USB Control Register Area cannot be mapped in IO Resource Area.



- LCD & Serial Port Control Register Area

As for accessing Resource in LCD & Serial Port Control Register Area, use Configuration Register Base Address Reg.(Config.offset: 10h) in LCD & Serial Port Host Controller for mapping the settings to access designated Memory Areas (800-FFFh). However, LCD & Serial Port Control Register Area cannot be mapped in IO Resource Area.



- Local Memory Area

This area can be used by setting LMEN bit(D0) of Internal Local Memory Enable Register(Config.offset:40h) in USB Host Controller Configuration Register. In the case of not used USB Host Controller, this area can be used as general memory area.

4.3 Register Map

Register map of each register of TC6391XB are shown.

4.3.1 System Configuration Register

31	23	15	07	00	Port
					00-07h
				Revision ID	08h
					0C-3Fh
	INT Mask				40h
					44-DFh
	Reserved 1		INT Status	Device Control	E0h
					E4-EFh
GPI Status			GPO Output Enable	GPO Output Control	F0h
					F4h
				Active pull-up/down Control	F8h
Reserved 3				Reserved 2	FCh

4.3.2 SD Host Controller Configuration Register

31 23	15 07	00	Port
Reserved 2	Reserved 1		00h
Reserved 3	Command		04h
Reserved 5		Reserved 4	08h
	Reserved 6		0Ch
SD Control Register Base Address			10h
			14h
			18h
			1Ch
			20h-2Bh
Reserved 8	Reserved 7		2Ch
			30h
		Reserved 9	34h
			38h
	Interrupt Pin	Reserved 10	3Ch
	Gated Clock Control	Stop Clock Control	40h
	Pin Status		44h
Power Control3	Power Control2	Power Control1	48h
	Reserved 11	Card Detect Mode	4Ch
		SD Slot	50h
			54h
	Reserved 12		58h
			5Ch
	Reserved 13		60h
			64h-7Fh
Reserved 16	Reserved 15	Reserved 14	80h
Reserved 19 Reserved 18	Reserved 17		84h
	Reserved 20		88h
			8C-EFh
Reserved 21	Extend Gated Clock Control2	Extend Gated Clock Control1	F0h
			F4h
Reserved 23	Extend Gated Clock Control3	Reserved 22	F8h
Reserved 26	Reserved 25	Reserved 24	FCh

4.3.3 SD Control Register

Base Address: SD Port Register Base Address (Conf.10h)

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	SD Control Reserved 1		000h	SD Command	
006h	Argument1		004h	Argument0	
00Ah	Transfer Sector Count		008h	Stop internal action	
00Eh	Response1		00Ch	Response0	
012h	Response3		010h	Response2	
016h	Response5		014h	Response4	
01Ah	Response7		018h	Response6	
01Eh	SD Buffer Control & Error Status		01Ch	SD Card Status	
022h	SD Interrupt Mask1		020h	SD Interrupt Mask0	
026h	SD Memory Card Transfer Data Length		024h	SD Card Clock Control	
02Ah	---		028h	SD Memory Card Option Setup	
02Eh	SD Error Detail Status 1		02Ch	SD Error Detail Status 0	
032h	---		030h	SD Data Port	
036h	---		034h	Transaction Control	
03Ah	---		038h	---	
03Eh	---		03Ch	---	
0E2h	SD Control Reserved 2		0E0h	SD Software Reset	
0E6h	SD Control Reserved 3		0E4h	---	
0EAh	---		0E8h	---	
0EEh	---		0ECh	---	
0F2h	---		0F0h	---	
0F6h	SD Control Reserved 4		0F4h	---	
0FAh	SD Control Reserved 6		0F8h	SD Control Reserved 5	
0FEh	SD Control Reserved 8		0FCh	SD Control Reserved 7	
102h	SD Card Port Selection		100h	SD Command	
106h	Argument1		104h	Argument0	
10Ah	Transfer Block Count		108h	---	
10Eh	Response1		10Ch	Response0	
112h	Response3		110h	Response2	
116h	Response5		114h	Response4	
11Ah	Response7		118h	Response6	
11Eh	SD Buffer Control & Error Status		11Ch	SD Card Status	
122h	SD Interrupt Mask1		120h	SD Interrupt Mask0	
126h	SDIO Card Transfer Data Length		124h	---	
12Ah	---		128h	SDIO Card Option Setup	
12Eh	SD Error Detail Status1		12Ch	SD Error Detail Status0	
132h	---		130h	SD Data Port	
136h	Card Interrupt Control		134h	Transaction Control	
13Ah	SDIO Host Information		138h	Clock & Wait Control	
13Eh	---		13Ch	Error Control	
1E2h	SD Control Reserved 9		1E0h	SD Software Reset	
1E6h	---		1E4h	---	
1EAh	---		1E8h	---	
1EEh	---		1ECh	---	
1F2h	---		1F0h	SD Control Reserved 10	
1F6h	---		1F4h	---	
1FAh	---		1F8h	---	
1FEh	---		1FCh	---	

4.3.4 SmartMedia™ Host Controller Configuration Register

31 23	15 07	00	Port
Reserved 2	Reserved 1		00h
Reserved 3	Command		04h
Reserved 5		Reserved 4	08h
Reserved 6			0Ch
SmartMedia™ Control Register Base Address			10h
			14h-27h
			28h
Reserved 8	Reserved 7		2Ch
			30h
		Reserved 9	34h
			38h
	Interrupt Pin	Reserved 10	3Ch
			40h-47h
Event Control	Reserved 11	INT Enable	48h
		Internal Clock Control	4Ch
			50h-57h
Debug			58h
			5Ch-5Fh
SmartMedia™ Detect Control	SmartMedia™ Power Supply Control	SmartMedia™ Monitor	SmartMedia™ Transaction Control	60h
			64h-7Fh
Reserved 14	Reserved 13	Reserved 12	80h
Reserved 17 Reserved 16	Reserved 15		84h
			88h-9Fh
			A0h-EFh
			F0h
			F4h-FBh
Reserved 19		Reserved 18	FCh

4.3.5 SmartMedia™ Control Register

Base Address: SmartMedia™ Controller Register Base Address (Conf.10h)

Offset	Register name	R/W
03h-00h	Data Register	RW
04h(Read/Write)	Mode Register	W(R/W)
05h	Status Register	R
06h	Interrupt Status Register	R
07h	Interrupt Mask Register	RW

4.3.6 USB Host Controller Configuration Register

31	23	15	07	00	Port
					00-07h
				Revision ID	08h
					0Ch
USB Control Register Base Address					10h
					14-3Fh
				Internal Local Memory Enable	40h
Local Memory Window 1 Base Address		Local Memory Window 1 LMADRS			44h
Local Memory Window 2 Base Address		Local Memory Window 2 LMADRS			48h
		Power Management			4Ch
				INT Control	50h
					54-F8h
					F8h
				MISC	FCh

4.3.7 USB Control Register

T.B.D

4.3.8 LCD & Serial Port Host Controller Configuration Register

31	23	15	07	00	Port
					00h
				Command	04h
				Revision ID	08h
					0Ch
		LCD & Serial Port Control Register Base Address			10h
					14-1Fh
		Clock Control			20h
					24-FFh

4.3.9 LCD & Serial Port Control Register

31	23	15	07	00	Port
		Revision Code			00h
		Interrupt Status			04h
					08h-1Fh
Xstart		Horizontal Total			20h
XST Start		XCK High Width			24h
Vertical Total		STH Start			28h
YST Start		YCK Start Wait			2Ch
PREC Width		#PPOL Start			30h
COM Output Control		VCLK High Width			34h
					38-5Fh
	SCC0 Frame Length		SCC0 Transmit/Receive Function		60h
SCC0 Interrupt Status (After Mask)			SCC0 Interrupt Status & Clear		64h
	SCC0 Transmit FIFO Control		SCC0 Communication Status		68h
	SCC0 Transmit/Receive FIFO Data		SCC0 Receive FIFO Control		6Ch
					70-7Fh
SCC1 Base Clock Control 1		SCC1 Base Clock Control 0			80h
	SCC1 Modem Status & Control		SCC1 Frame Control		84h
	SCC1 FIFO Control		SCC1 FIFO Data		88h
	SCC1 Interrupt Status		SCC1 Line Control		8Ch
	SCC1 Interrupt Clear	SCC1 Interrupt Control			90h
					94-9Fh
SCC2 Base Clock Control 1		SCC2 Base Clock Control 0			A0h
	SCC2 Modem Status & Control		SCC2 Frame Control		A4h
	SCC2 FIFO Control		SCC2 FIFO Data		A8h
	SCC2 Interrupt Status		SCC2 Line Control		ACh
	SCC2 Interrupt Clear	SCC2 Interrupt Control			B0h
					B4-FFh

4.4 Clock/Reset

4.4.1 Clock

TC6391XB holds the following three Input Clock Pins: HCLK, CK48M, CLK32

(1) HCLK : System Clock Input (Max.33MHz).
Basic Clock for System Interface and internal operations.

(2) CK48M : External Clock Input(Max.48MHz)
Basic Clock for USB and Serial Port interfaces.

(3) CLK32 : Clock Input for 32KHz. The interrupt signal, implied for insertion and detachment of a SD card shall be generated synchronous to this signal. In addition, this signal is base clock, which input to a register which set timeout error time on SD data from a SDIO card.

4.4.2 Reset-related items

- #PCLR: Reset Signal is asserted when power is supplied.
All registers(built into TC6391XB) are cleared by #PCLR.

Be sure to deactivate assertion of #PCLR when power supply and HCLK oscillation (better than 1ms) are fairly stable.

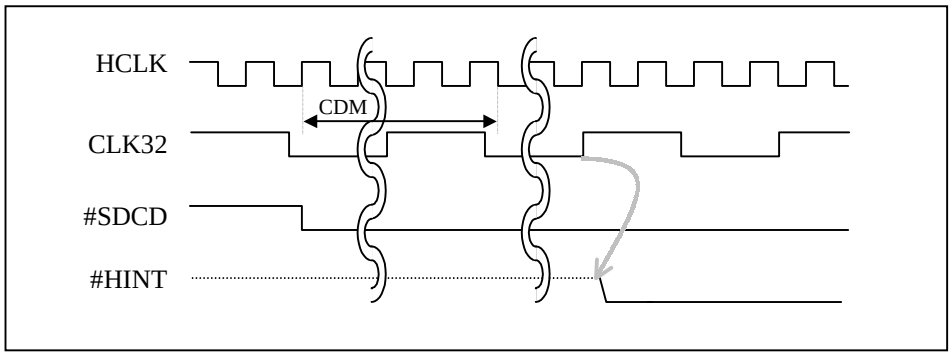
4.5 SD card interrupt

When the TC6391XB detects the each interrupt sources from a SD card, TC6391XB asserts interrupt signals (#HINT). It is necessary that the interrupt mask bits are released. This mask bits releasing is controlled by setting SD Interrupt Mask Register(Offset:020-023h, 120-123h). Each factor of the interrupt can be evaluated by referring to SD Card Status Register(Offset:01C-01Dh, 11C-11Dh) or SD Buffer Control & Error Status Register(Offset:01E-01Fh, 11E-11Fh). The details of each factor are listed below.

4.5.1 SD card insertion interrupt by #SDCD

+ Interrupt Assert Condition

When an SD card is inserted to a slot, #SDCD is lowered. This condition causes an interrupt to be generated. #SDCD is not recognized as being lowered unless it remains in "0" state for the number of CLK32 cycles specified by CDM[1:0] of Card Detect Mode Register(Config Offset:4Ch). The interrupt is asserted in th timing of raising of CLK32 from #SDCD low state.



+ Factor Evaluation Method

The SCIN bit(D4) of SD Card Status Register(Offset:01C-01Dh) is set to "1".

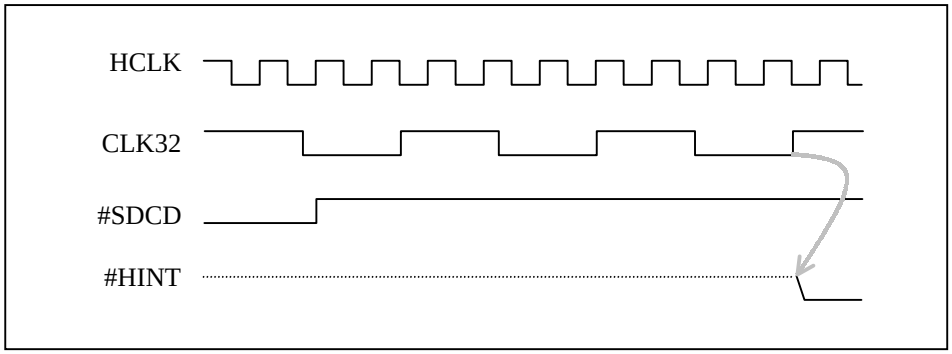
+De-asserting Method

(1) "0" is written into the SCIN bit(D4) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MCIN bit(D4) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

4.5.2 SD card removal interrupt by #SDCD

+ Interrupt Assert Condition

When an SD card in a slot is removed, #SDCD is raised. This condition causes an interrupt to be generated. After #SDCD is high, the interrupt is asserted in th timing of raising of CLK32.



+ Factor Evaluation Method

The SCOT bit(D3) of SD Card Status Register(Offset:01C-01Dh) is set to "1".

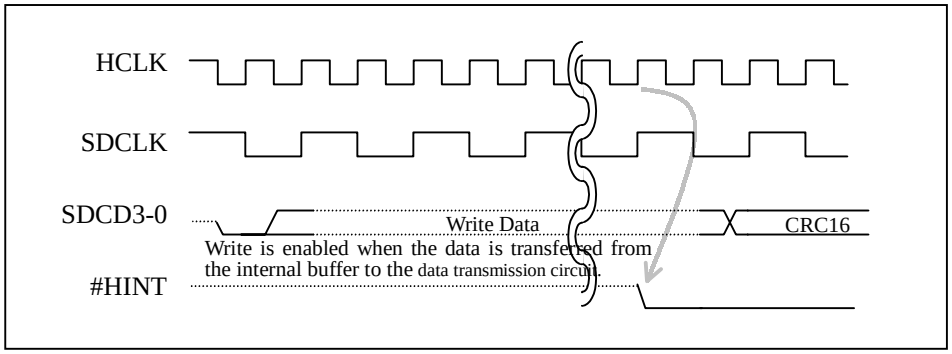
+De-asserting Method

(1) "0" is written into the SCOT bit(D3) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MCOT bit(D3) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

4.5.3 Buffer write enable interrupt

+ Interrupt Assert Condition

When data to be transmitted to the card becomes available for the internal buffer, SD Data Port Register(Offset:030-031h, 130-131h), to be written for a write command, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MBWE bit(D25) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

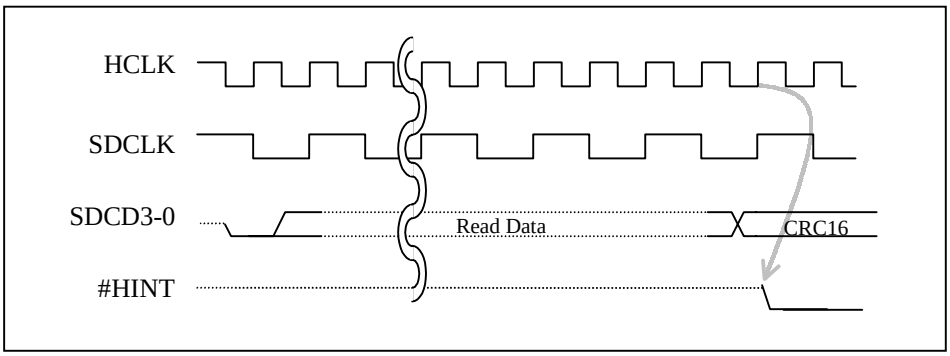
SDIO Card

(1) "0" is written into the SBWE bit(D9) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MBWE bit(D25) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.4 Buffer read enable interrupt

+ Interrupt Assert Condition

When one block of data from the card is stored fully into the internal buffer for a read command, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MBRE bit(D24) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

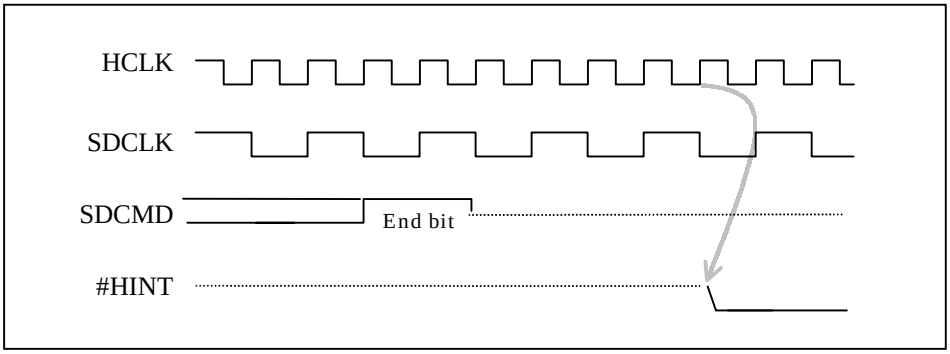
(1)"0" is written into the SBRE bit(D8) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MBRE bit(D24) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.5 Response end interrupt

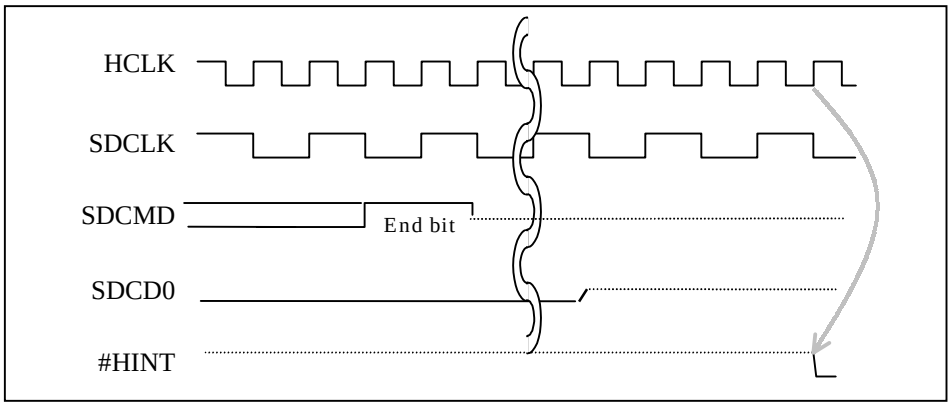
+ Interrupt Assert Condition

After a response received from an SD card, an interrupt is generated. Regarding R1b response type, after busy released from an SD card, an interrupt is generated.

<In the case of normal command>



<In the case of R1b command>



+ Factor Evaluation Method

In the case of SD memory Card, the SREP bit(D0) of SD Card Status Register(Offset:01C-01Dh) is set to "1". In the case of SDIO Card, the SREP bit(D0) of SD Card Status Register(Offset:11C-11Dh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SREP bit(D0) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MREP bit(D0) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

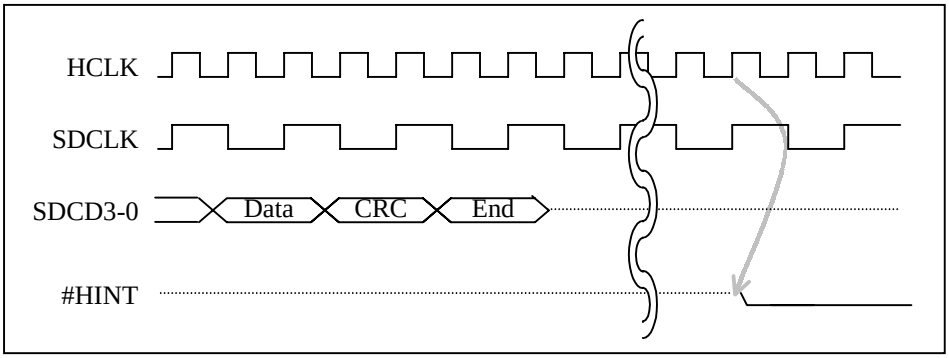
(1) "0" is written into the SREP bit(D0) of SD Card Status Register(Offset:11C-11Dh)
(2) "1" is written into the MREP bit(D0) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.6 R/W end interrupt

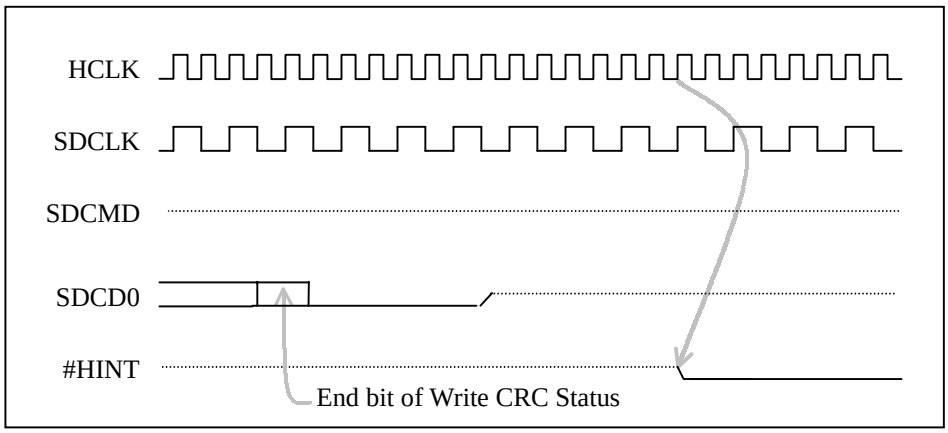
+ Interrupt Assert Condition

When read or write processing for an SD card is completed, an interrupt is generated.

<In the case of read command>



<In the case of write command>



+ Factor Evaluation Method

In the case of SD memory Card, the SRWA bit(D2) of SD Card Status Register(Offset:01C-01Dh) is set to "1". In the case of SDIO Card, the SRWA bit(D2) of SD Card Status Register(Offset:11C-11Dh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SRWA bit(D2) of SD Card Status Register(Offset:01C-01Dh).
(2) "1" is written into the MRWA bit(D2) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

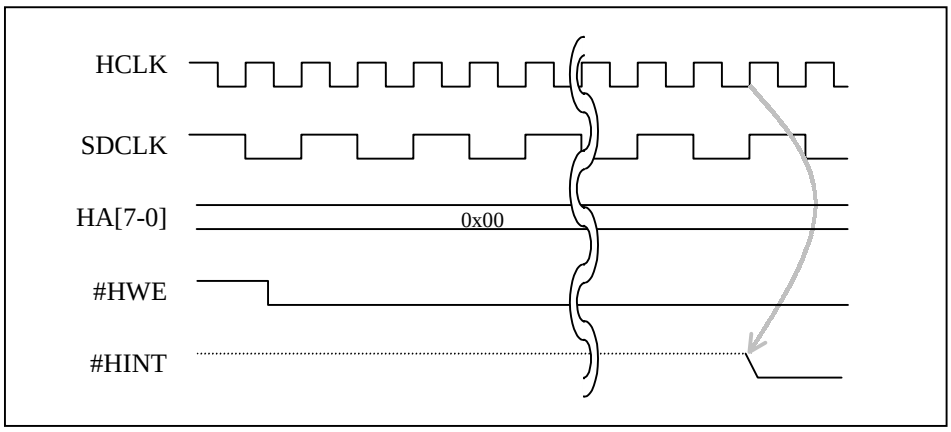
(1) "0" is written into the SRWA bit(D2) of SD Card Status Register(Offset:11C-11Dh)
(2) "1" is written into the MRWA bit(D2) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.7 Illegal access error interrupt

+ Interrupt Assert Condition

When an incorrect command index is written into SD Command Register(Offset:000-001h, 100-101h), an interrupt is generated. Each of the following cases is recognized as an incorrect index. (3) is only applying to SD memory Card.

(1) SD Command Register is written before the previously issued command is not completed.
(2) Though the REP2-0 bits(D10-8) are set to 011b(no response), the NTDT bit(D11) is set to 1b(with data).
(3) Though the CMD1-0 bits(D7-6) are set to 00b and the CIX bits(D5-0) are set to 001100b(CMD12), the NTDT bit(D11) is set to 1b(with data).



+ Factor Evaluation Method

In the case of SD memory Card, the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the IMSK bit(D31) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

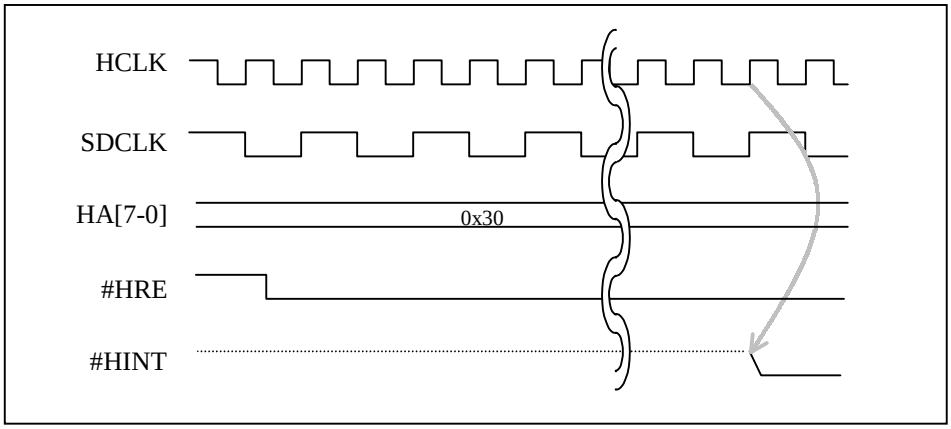
SDIO Card

(1) "0" is written into the ILA bit(D15) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the IMSK bit(D31) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.8 Buffer underflow error interrupt

+ Interrupt Assert Condition

If the host reads SD Data Port Register when the data buffer is empty, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset: 11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MFUF bit(D21) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

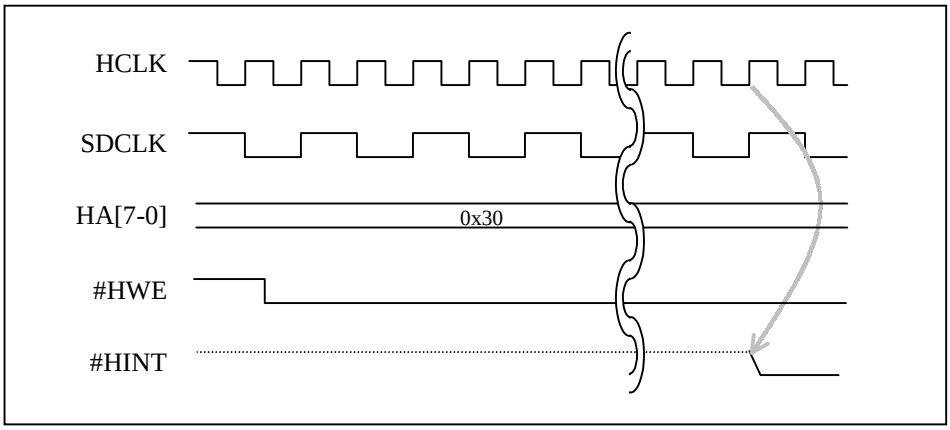
SDIO Card

(1) "0" is written into the SFUF bit(D5) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MFUF bit(D21) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.9 Buffer overflow error interrupt

+ Interrupt Assert Condition

If the host writes SD Data Port Register when the data buffer is full, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) is set to "1". In the case of SDIO Card, the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset: 11E-11Fh) is set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MFOF bit(D20) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

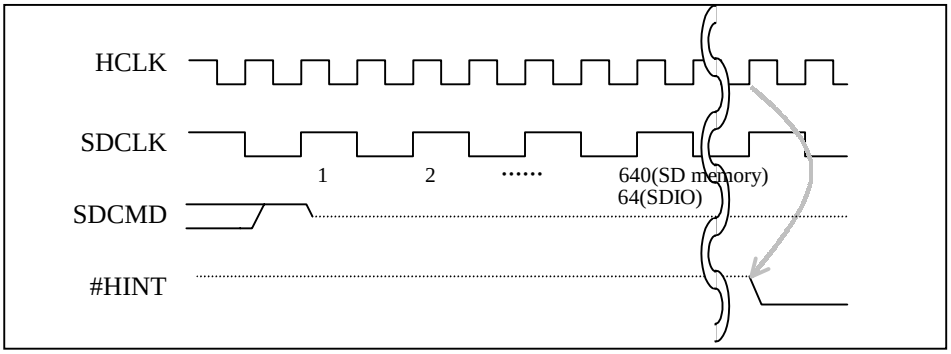
SDIO Card

(1) "0" is written into the SFOF bit(D4) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MFOF bit(D20) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.10 Time out error(command) interrupt

+ Interrupt Assert Condition

If the start bit of a response is not received within SDCLK period X 640(SD memory Card) or X 64(SDIO Card) after the end bit of a command is transmitted to the card, this condition is considered a time out error and an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NCR bit(D16) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1". However, if a response for automatically issued CMD12 is not received, the NRS bit(D17) is set to "1" for differentiation.

In the case of SDIO Card, the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NCR bit(D16) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCTO bit(D22) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

(1) "0" is written into the SCTO bit(D6) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCTO bit(D22) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

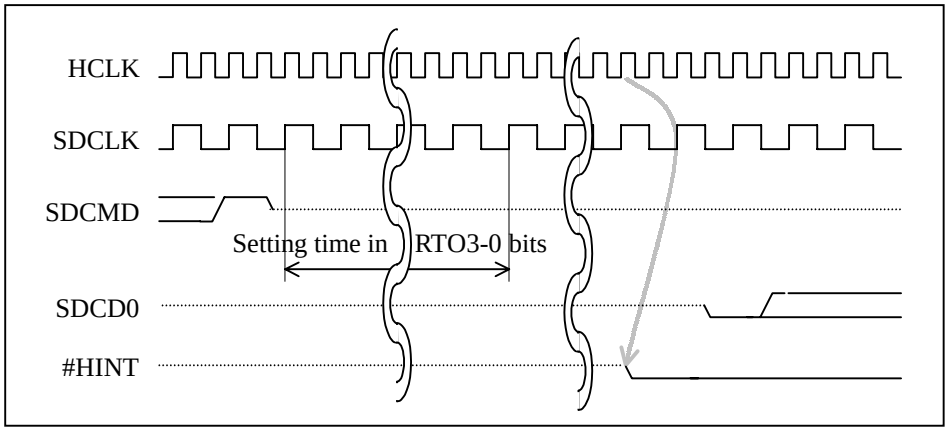
4.5.11 Read data time out error interrupt

+ Interrupt Assert Condition

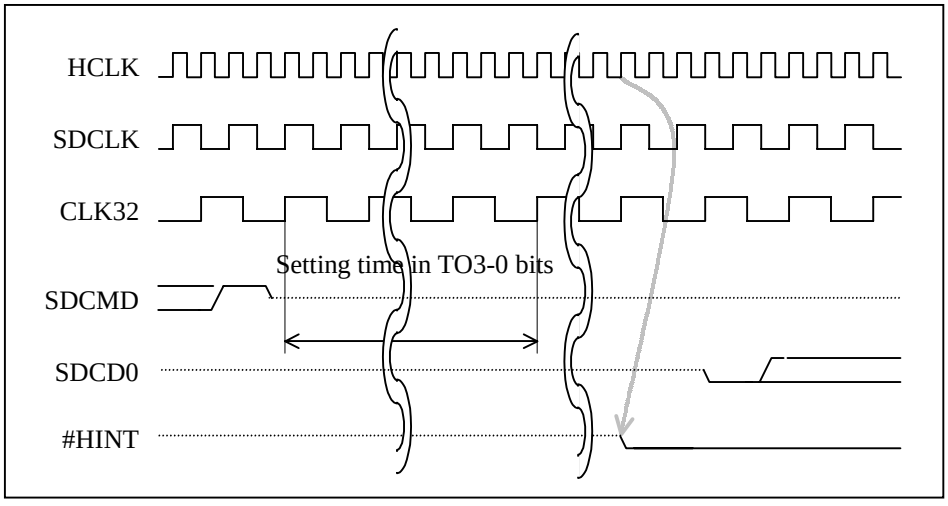
If the start bit of data is not detected within the specified period after the end bit of a response for each read command, an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period. Read data time out error is classified into between a command and a read data, and between a read data and a read data in a multiple block transfer.

*Between a command and a read data, time out

<In the case of SD memory card>

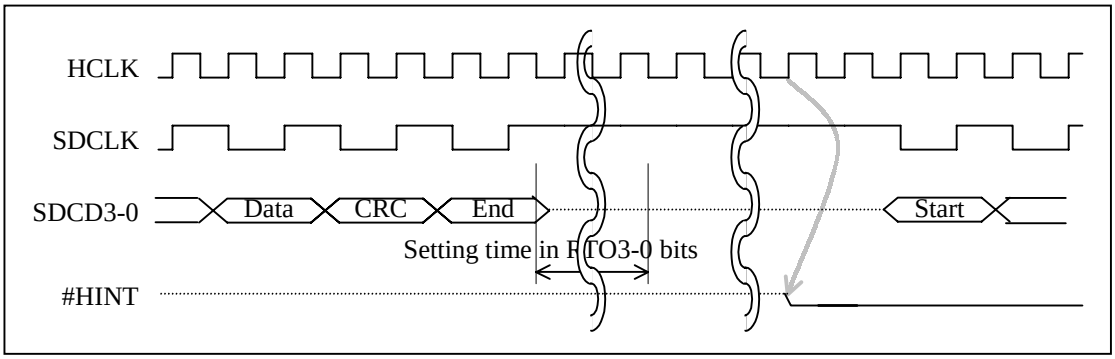


<In the case of SDIO card>

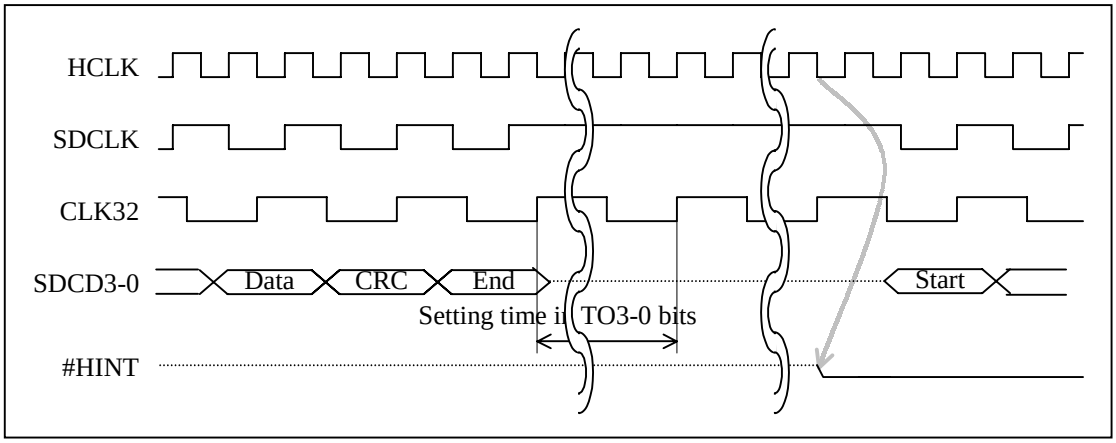


*Between a read data and a read data, time out

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

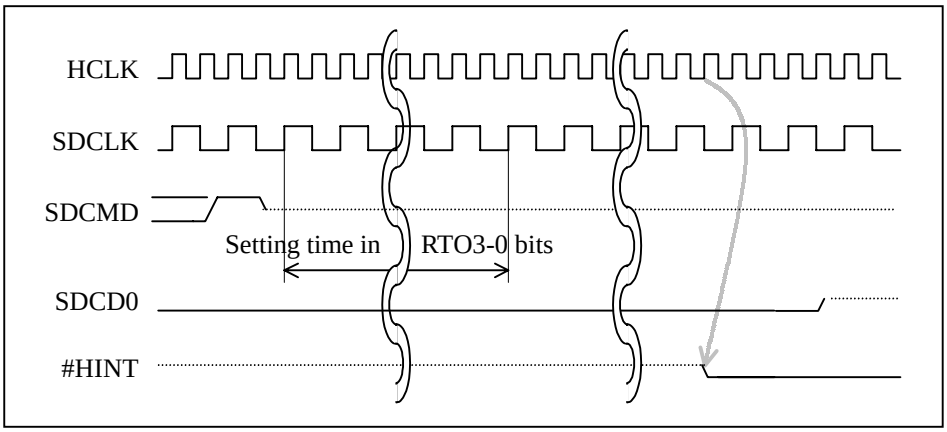
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.12 Busy time out error interrupt

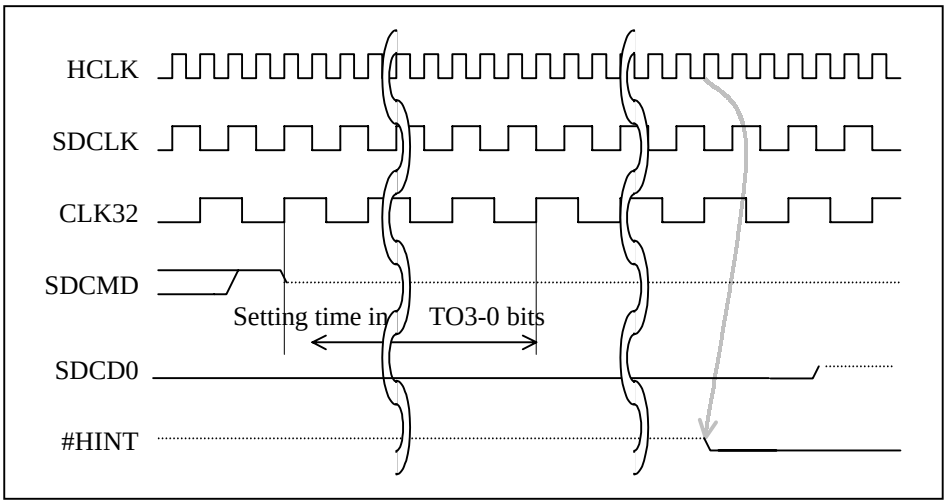
+ Interrupt Assert Condition

If a busy declaration from the card (DAT0 = "0" after response end) remains longer than the specified time, this condition is considered as a time out error and an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NRCS bit(D20) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

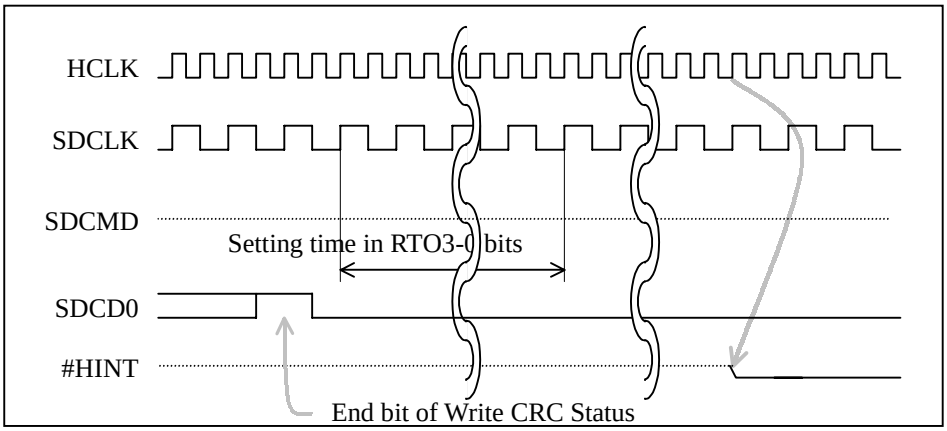
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.13 CRC status busy time out error interrupt

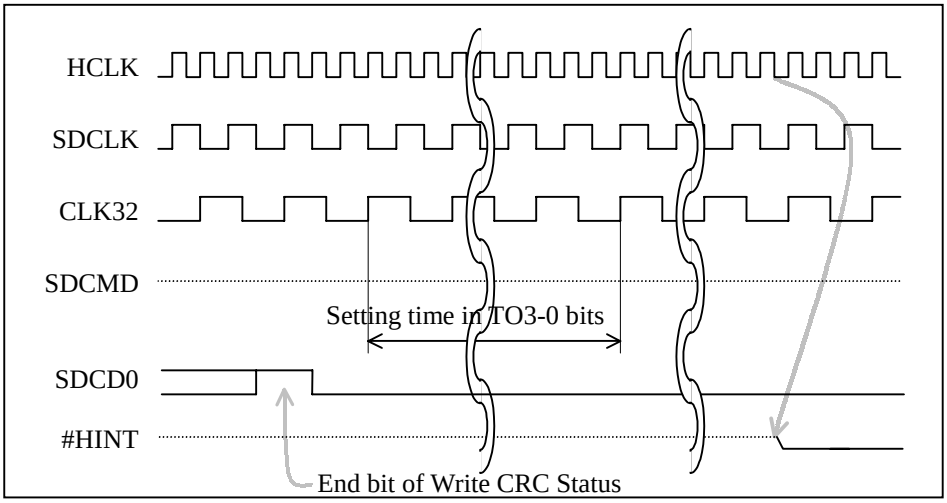
+ Interrupt Assert Condition

If a busy declaration from the card (DAT0 = "0" after Write CRC Status) remains longer than the specified time, this condition is considered as a time out error and an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the KBSY bit(D22) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the KBSY bit(D22) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

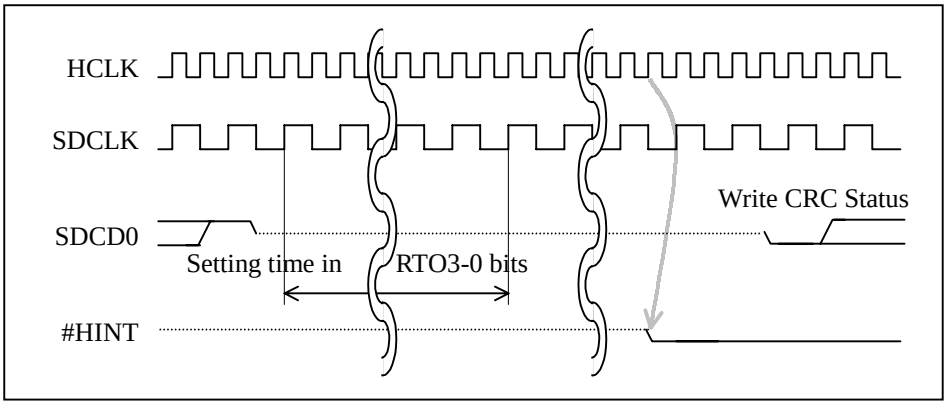
(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.14 CRC status time out error interrupt

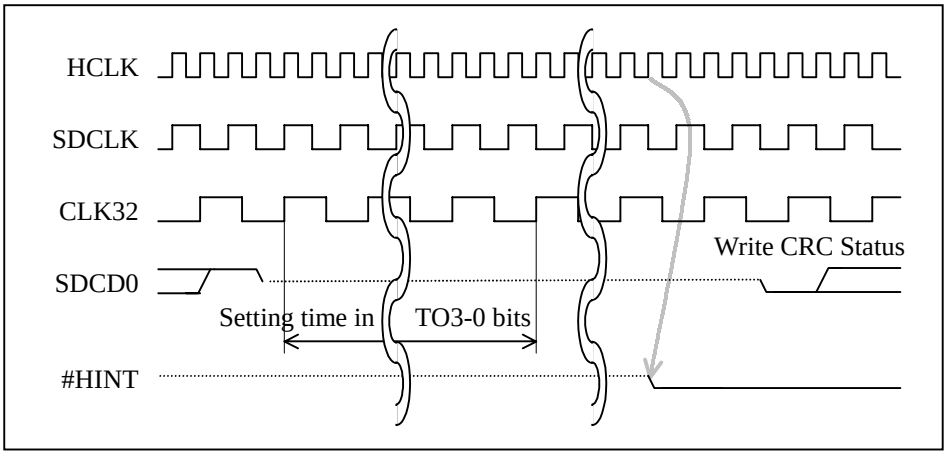
+ Interrupt Assert Condition

If the start bit of CRC status is not detected within the specified period after the end bit of block data for a write command, an interrupt is generated. In the case of SD memory Card, the specified period is set in RTO[3:0] of SD Memory Card Option Setup Register(Offset:028h) in the form of a multiple number of the SDCLK period. In the case of SDIO Card, the specified period is set in TO[3:0] of SD Memory Card Option Setup Register(Offset:128h) in the form of a multiple number of the CLK32 period.

<In the case of SD memory card>



<In the case of SDIO card>



+ Factor Evaluation Method

In the case of SD memory Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the NWCS bit(D21) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the NWCS bit(D21) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

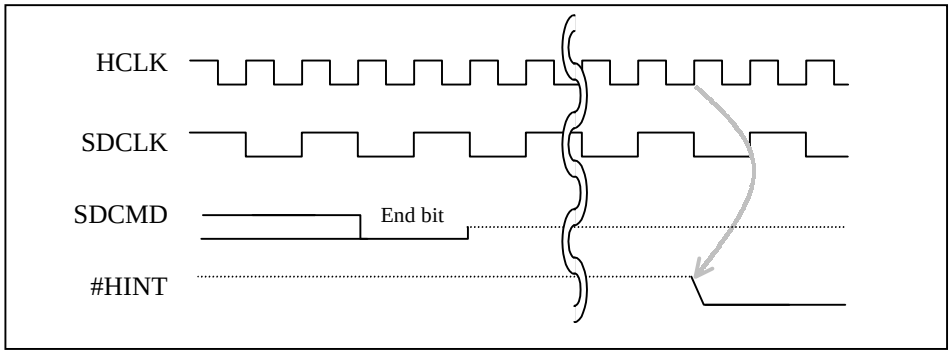
SDIO Card

(1) "0" is written into the SDTO bit(D3) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MDTO bit(D19) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.15 End bit error interrupt

+ Interrupt Assert Condition

If a bit that should be the end bit for the response, read data or CRC status received from the card is "0", an interrupt for detecting an incorrect end bit is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the WEBER bit, REBER bit, SEBER bit and CEBER bit(D5-2) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the WEBER bit, REBER bit and CEBER bit(D5-4,2) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

Bit	Name	Error factor	Notes
5	WEBER	End bit error for Write CRC status	
4	REBER	End bit error for read data	
3	SEBER	End bit error of a response for automatically issued CMD12	Only SD memory Card
2	CEBER	End bit error for a response (other than SEBER)	

+De-asserting Method

SD memory Card

(1) "0" is written into the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MEND bit(D18) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

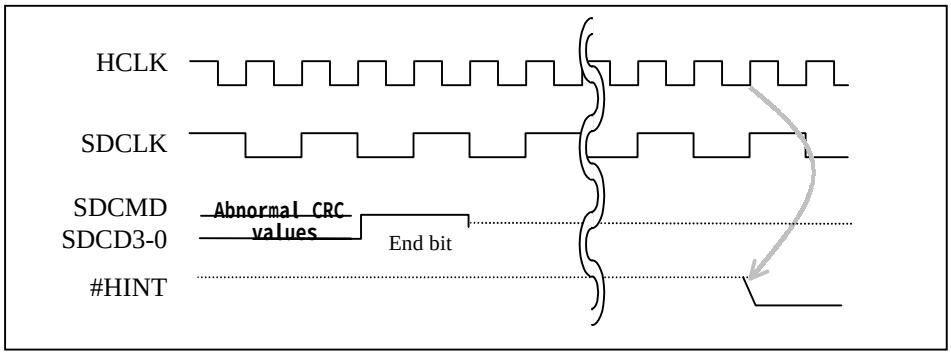
SDIO Card

(1) "0" is written into the SEND bit(D2) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MEND bit(D18) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.16 CRC error interrupt

+ Interrupt Assert Condition

If the CRC value for the response, read data or CRC status received from the card does not agree with the value internally calculated by TC6391XB, an interrupt is generated



+ Factor Evaluation Method

In the case of SD memory Card, the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the WCRCE bit, RCRCE bit, SCRCE bit and CCRCE bit(D11-8) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1".

In the case of SDIO Card, the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the WCRCE bit, RCRCE bit and CCRCE bit(D11-10,8) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

Bit	Name	Error factor	Notes
11	WCRCE	Write CRC status error for a write command	
10	RCRCE	CRC error for read data	
9	SCRCE	CRC error of a response for automatically issued CMD12	Only SD memory Card
8	CCRCE	CRC error for a response (other than SCRCE)	

+De-asserting Method

SD memory Card

(1) "0" is written into the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCRC bit(D17) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

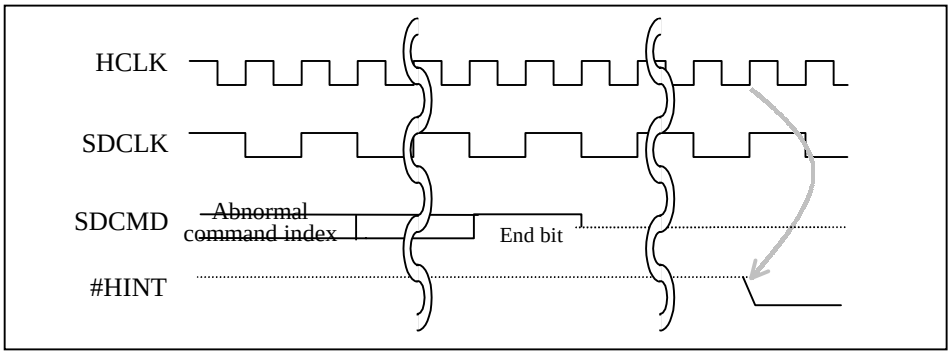
SDIO Card

(1) "0" is written into the SCRC bit(D1) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCRC bit(D17) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.17 Command Index error interrupt

+ Interrupt Assert Condition

If the command index portion of the response received from the card does not agree with the index issued just before, an interrupt is generated.



+ Factor Evaluation Method

In the case of SD memory Card, the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:01E-01Fh) and the RCMDE bit(D0) of SD Error Detail Status Register(Offset:02C-02Fh) are set to "1". If a response for automatically issued CMD12 is not normal, "1" is set to the SCMDE bit(D0).

In the case of SDIO Card, the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) and the RCMDE bit(D0) of SD Error Detail Status Register(Offset:12C-12Fh) are set to "1".

+De-asserting Method

SD memory Card

(1) "0" is written into the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:01E-01Fh).
(2) "1" is written into the MCIX bit(D16) of SD Interrupt Mask Register(Offset:020-023h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:0E0h).

SDIO Card

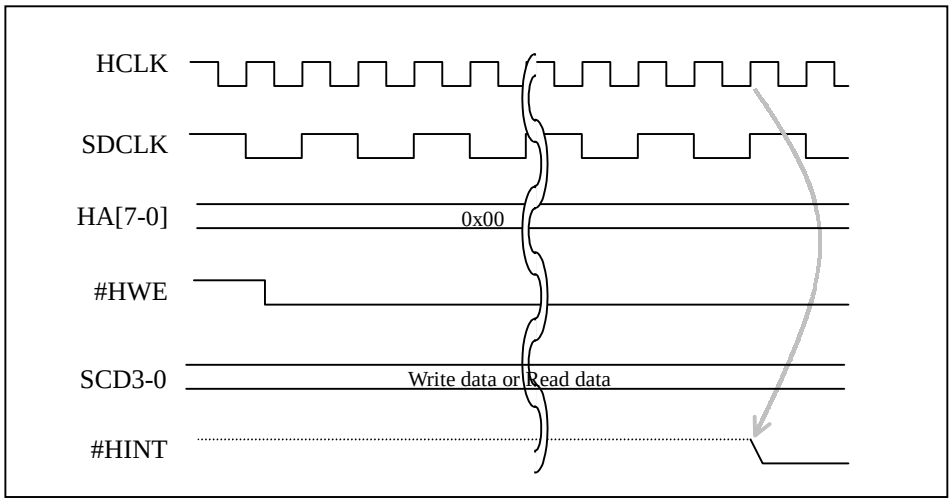
(1) "0" is written into the SCIX bit(D0) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the MCIX bit(D16) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.18 Illegal function select interrupt

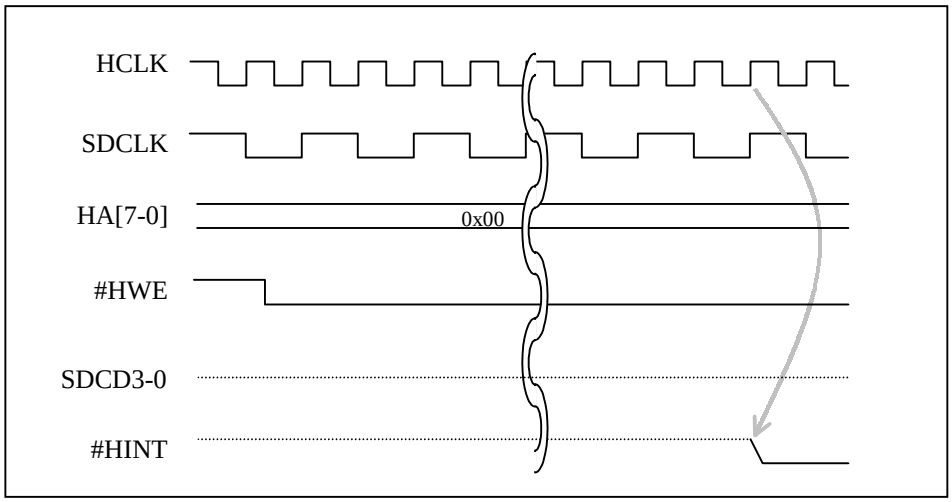
+ Interrupt Assert Condition

Although a transaction is remaining on the SD bus, or a state of SD controller is acceptable, SD host controller selects other function in SDIO Card, and then an interrupt is generated.

<In the case of remaining transaction on the SD bus>



<In the case of SD controller is an acceptable state>



+ Factor Evaluation Method

The ILFSL bit(D13) of SD Buffer Control & Error Status Register(Offset:11E-11Fh) is set to "1".

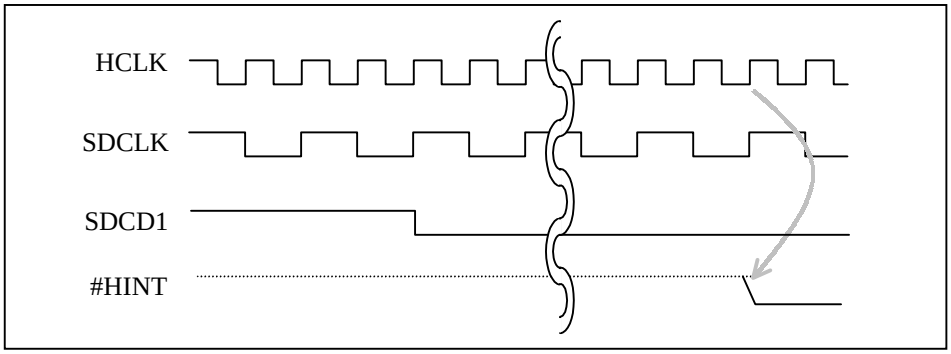
+De-asserting Method

(1) "0" is written into the ILFSL bit(D13) of SD Buffer Control & Error Status Register(Offset:11E-11Fh).
(2) "1" is written into the IFSMSK bit(D29) of SD Interrupt Mask Register(Offset:120-123h).
(3) Hardware reset by #PCLR = “0”.
(4) Software reset by writing "0" into the SRST bit(D0) of SD Software Reset Register(Offset:1E0h).

4.5.19 SDIO Card interrupt

+ Interrupt Assert Condition

When an interrupt from SDIO Card by using SDCD1 signal is detected, an interrupt is generated. Please release the interrupt mask by the CIMSK0 bit(D8) of Card Interrupt Control Register(Offset:136h), so the interrupt from #HINT would be generated.



+ Factor Evaluation Method

The CINT0 bit(D12) of Card Interrupt Control Register(Offset:136h) is set to "1".

+De-asserting Method

(1) "0" is written into the CINT0 bit(D12) of Card Interrupt Control Register(Offset:136h).
(2) "1" is written into the CIMSK0 bit(D8) of Card Interrupt Control Register(Offset:136h).
(3) Hardware reset by #PCLR = “0”.

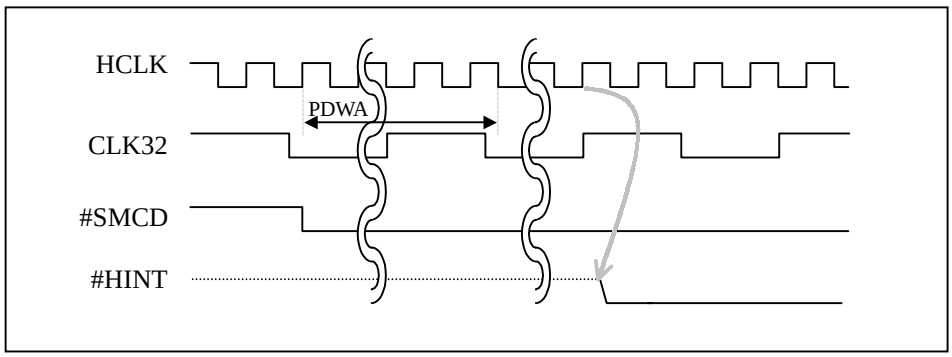
4.6 SmartMedia interrupt

When the TC6391XB detects the each interrupt sources from SmartMedia card, TC6391XB asserts interrupt signals (#HINT). It is necessary that the interrupt output is enabling and the interrupt mask bits are released. Interrupt enabling is controlled by setting D7 of Interrupt Mask Register(Offset:07h). And, mask bits releasing is controlled by setting D3-0 of Interrupt Mask Register(Offset:07h). Each factor of the interrupt can be evaluated by referring to Interrupt Status Register(Offset:06h).

4.6.1 SmartMedia insertion interrupt by #SMCD

+ Interrupt Assert Condition

When a SmartMedia card is inserted to a slot, #SMCD is lowered. This condition causes an interrupt to be generated. #SMCD is not recognized as being lowered unless it remains in "0" state for the number of HCLK cycles specified by PDWA[1:0] of SmartMedia Detect Control Register(Config Offset:63h). The interrupt is asserted in th timing of raising of HCLK from #SMCD low state.



+ Factor Evaluation Method

The CDIN bit(D3) of Interrupt Status Register(Offset:06h) is set to "1".

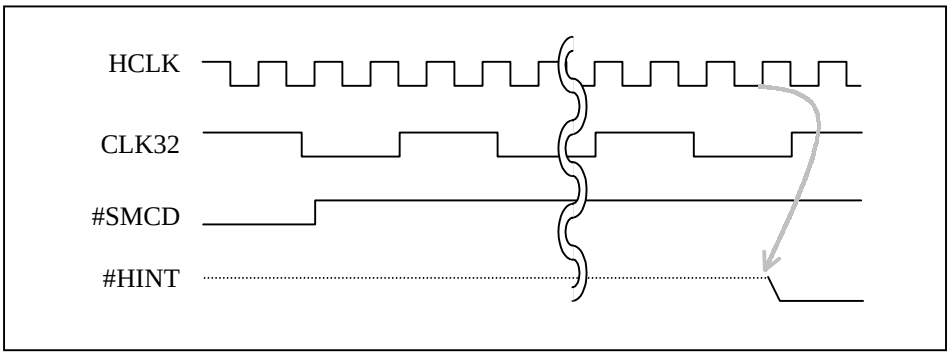
+De-asserting Method

(1)"1" is written into the CDIN bit(D3) of Interrupt Status Register(Offset:06h).
(2) "0" is written into the INTEN bit(D7) of Interrupt Mask Register(Offset:07h).
(3) "0" is written into the MCDIN bit(D3) of Interrupt Mask Register(Offset:07h).
(4) Hardware reset by #PCLR = “0”.

4.6.2 SmartMedia removal interrupt by #SMCD

+ Interrupt Assert Condition

When a SmartMeida card in a slot is removed, #SMCD is raised. This condition causes an interrupt to be generated. After #SMCD is high, the interrupt is asserted in th timing of raising of HCLK.



+ Factor Evaluation Method

The CDOUT bit(D2) of Interrupt Status Register(Offset:06h) is set to "1".

+De-asserting Method

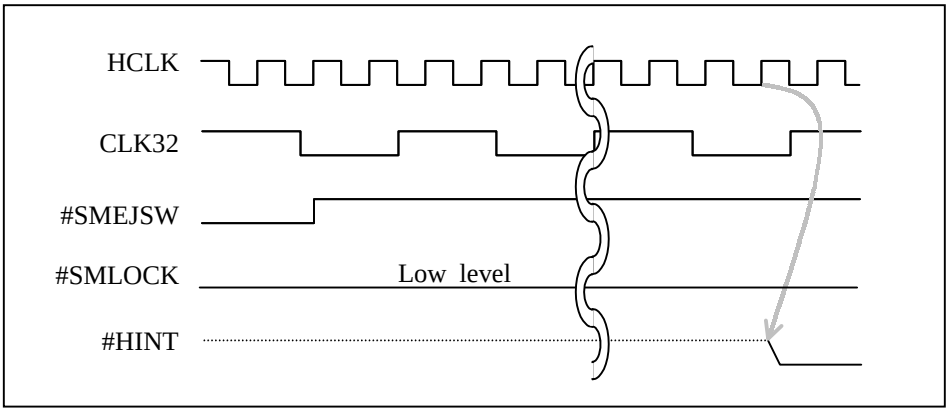
(1)"1" is written into the CDOUT bit(D2) of Interrupt Status Register(Offset:06h).
(2) "0" is written into the INTEN bit(D7) of Interrupt Mask Register(Offset:07h).
(3) "0" is written into the MCDOUT bit(D2) of Interrupt Mask Register(Offset:07h).
(4) Hardware reset by #PCLR = “0”.

4.6.3 Interrupt by #SMEJSW signal

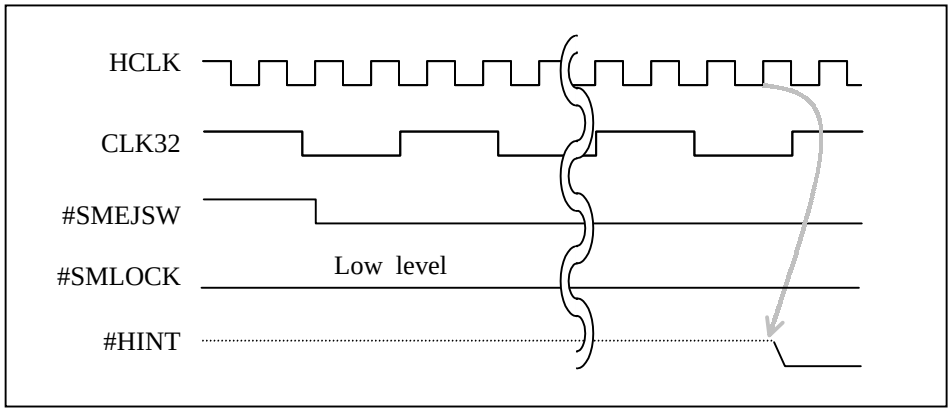
+ Interrupt Assert Condition

The level of #SMEJSW changes. This condition causes an interrupt to be generated. It is possible that a polarity of #SMEJSW is controlled by setting SEJINV bit of SmartMedia Detect Control Register(Config Offset:63h).

<In the case of SEJIEV bit=0b>



<In the case of SEJIEV bit=1b>



+ Factor Evaluation Method

The EJREQ bit(D1) of Interrupt Status Register(Offset:06h) is set to "1".

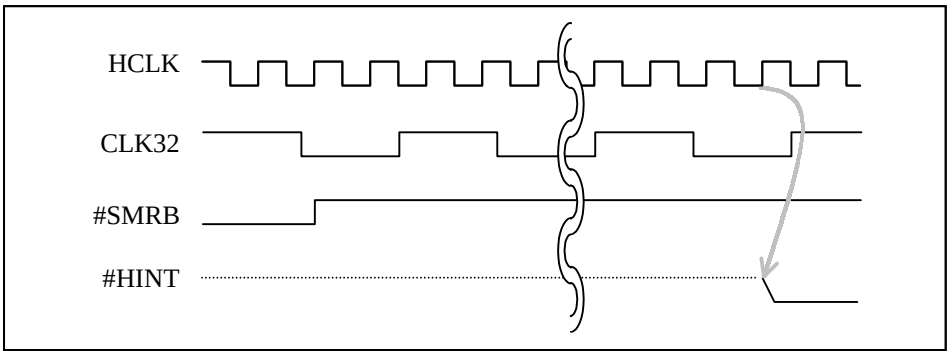
+De-asserting Method

(1)"1" is written into the EJREQ bit(D1) of Interrupt Status Register(Offset:06h).
(2) "0" is written into the INTEN bit(D7) of Interrupt Mask Register(Offset:07h).
(3) "0" is written into the MEJREQ bit(D1) of Interrupt Mask Register(Offset:07h).
(4) Hardware reset by #PCLR = “0”.

4.6.4 Interrupt when #SMRB signal changes from Low to High

+ Interrupt Assert Condition

The level of #SMRB changes from low to high. This condition causes an interrupt to be generated.



+ Factor Evaluation Method

The RDYREQ bit(D0) of Interrupt Status Register(Offset:06h) is set to "1".

+De-asserting Method

(1)"1" is written into the RDYREQ bit(D0) of Interrupt Status Register(Offset:06h).

(2) "0" is written into the INTEN bit(D7) of Interrupt Mask Register(Offset:07h).

(3) "0" is written into the MRDYREQ bit(D0) of Interrupt Mask Register(Offset:07h).

(4) Hardware reset by #PCLR = “0”.

4.7 USB interrupt

When the TC6391XB detects the each interrupt sources from USB device, TC6391XB asserts interrupt signals (#HINT). The details of each factor are listed below.

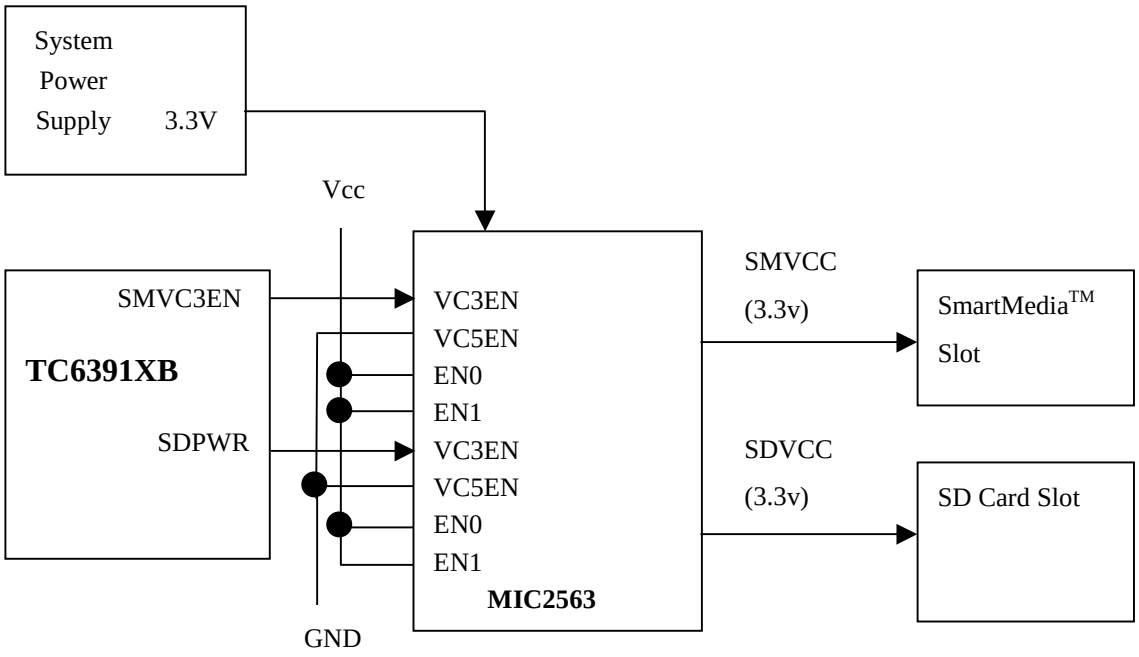
*Interrupt by insertion USB device
*Interrupt by removal USB device

4.8 Communication with serial port interface interrupt

When the TC6391XB detects the each interrupt sources from the communication with serial port interface, TC6391XB asserts interrupt signals (#HINT).

4.9 Card Slot Power Supply Control

TC6391XB can control power supply of a card slot of a SD card or SmartMedia, and a connector of USB device. The following suggests applicable circuits:



4.9.1 SD Card Slot Power Supply Controller

Power supply for SD Card is controlled by configuring Power Control Register 2(Config Offset 49h) after detecting SD Card insertion. When #SUSPEND is asserted to low, power supply for SD Card can be automatically shut out by configuring Power Control Register 3(Config Offset 4Ah).

Power Supply Control Signals

Signal Name	Function/Remarks	Pin
SDPWR	SD Card Slot Power Supply Controller. 3.3V Enable Signal	C6

4.9.2 SmartMedia™ Slot Power Supply Control

There are two modes for controlling power supply to the SmartMedia™ slot: Manual Power Supply Control mode and Automatic Power Supply Control mode. Those modes are switched using the bit 7 of the SmartMedia™ host controller configuration register at 62h. In Manual Power Supply Control mode, bits 3 and 2 of the SmartMedia™ control register (offset: 02h) are used. In Automatic Power Supply Control mode, when the SmartMedia™ is inserted, power is automatically turned on. When the SmartMedia™ is removed, power is turned off.

Power Supply Control Signal

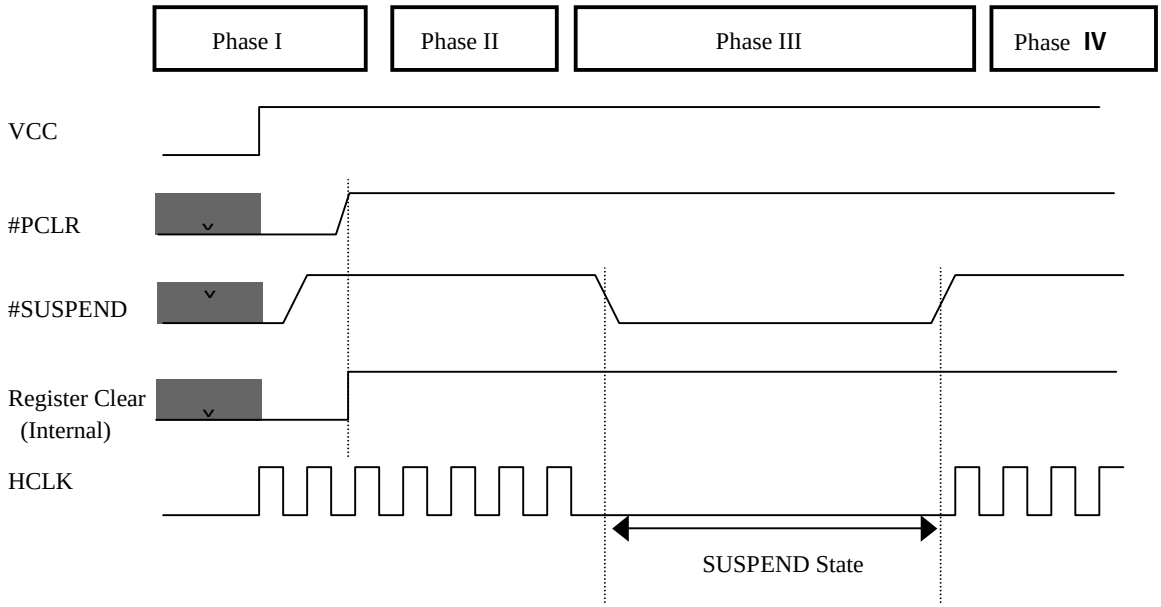
Signal Name	Function/Remarks	Pin
SMVC3EN	Controls VDD 3.3V for SmartMedia™	M9

4.9.3 USB device Connector Power Supply Control

T.B.D

4.10 Suspend

TC6391XB executes buffer-off for Input Signals by asserting #SUSPEND.



* Phase I: Immediately after the power is turned ON, #PCLR indicates "L" whereas #SUSPEND indicates "H". All the circuits are cleared in this state.
* Phase II: Assertion of #PCLR deactivated (H). Normal state.
* Phase III: Assert #SUSPEND to activate SUSPEND state. TC6391XB executes Anti-Penetration Process for Input Signals in this state. Also, TC6391XB does not accept Host Interface transactions in this state. Moreover, stopping HCLK can reduce the power consumption.
* Phase IV: TC6391XB is brought back to normal state by deactivating assertion of #SUSPEND.

It shows what state each signals are in suspend mode (#SUSPEND=Low).

NAME	Pin	IO	State	NAME	Pin	IO	State
HD15	J14	IO	Hi-Z	SDLED	C5	O	L
HD14	J15	IO	Hi-Z	SDPWR	C6	O	*
HD13	K13	IO	Hi-Z	SMD7	P4	IO	Hi-Z
HD12	K14	IO	Hi-Z	SMD6	P5	IO	Hi-Z
HD11	K15	IO	Hi-Z	SMD5	P6	IO	Hi-Z
HD10	L12	IO	Hi-Z	SMD4	P7	IO	Hi-Z
HD9	L13	IO	Hi-Z	SMD3	P8	IO	Hi-Z
HD8	L14	IO	Hi-Z	SMD2	P9	IO	Hi-Z
HD7	L15	IO	Hi-Z	SMD1	N9	IO	Hi-Z
HD6	M13	IO	Hi-Z	SMD0	N10	IO	Hi-Z
HD5	M14	IO	Hi-Z	SMCLE	N3	O	Hi-Z
HD4	M15	IO	Hi-Z	SMALE	N4	O	Hi-Z
HD3	N13	IO	Hi-Z	#SMCE	N7	O	Hi-Z
HD2	N14	IO	Hi-Z	#SMWE	N5	O	Hi-Z
HD1	N15	IO	Hi-Z	#SMRE	N6	O	Hi-Z
HD0	P15	IO	Hi-Z	#SMWP	N8	O	Hi-Z
HA13	D14	I	Hi-Z	#SMRB	M10	I	-
HA12	F14	I	Hi-Z	#SMCD	M11	I	-
HA11	F15	I	Hi-Z	SMLVD	M12	I	-
HA10	G12	I	Hi-Z	#SMWPD	N11	I	-
HA9	G13	I	Hi-Z	#SMEJSW	N12	I	-
HA8	G14	I	Hi-Z	#SMLED	M6	O(OD)	Hi-Z
HA7	G15	I	Hi-Z	#SMLOCK	M7	O(OD)	Hi-Z
HA6	H12	I	Hi-Z	#SMEJCT	M8	O(OD)	Hi-Z
HA5	H13	I	Hi-Z	SMVC3EN	M9	O	*
HA4	H14	I	Hi-Z	USB1DP	B3	IO	Hi-Z
HA3	H15	I	Hi-Z	USB1DN	A2	IO	Hi-Z
HA2	J12	I	Hi-Z	USB2DP	C3	IO	Hi-Z
HA1	J13	I	Hi-Z	USB2DN	B1	IO	Hi-Z
#HCS	F13	I	Hi-Z	USB3DP	C1	IO	Hi-Z
#HOE	F12	I	Hi-Z	USB3DN	D2	IO	Hi-Z
#HWE	E15	I	Hi-Z	PPON1	B4	O	*
#HBEL	E14	I	Hi-Z	PPON2	C4	O	*
#HBEH	E13	I	Hi-Z	PPON3	D5	O	*
HRDY	E11	O(OD)	Hi-Z	#USBOC	A3	I	-
SDCD3	A5	IO	Hi-Z	TXD0	R2	O	Hi-Z
SDCD2	A6	IO	Hi-Z	RXD0	R3	I	Hi-Z
SDCD1	A7	IO	Hi-Z	FRM0	R4	I	-
SDCD0	A8	IO	Hi-Z	SCK0	R5	I	-
SDCMD	B5	IO	Hi-Z	TXD1	R6	O	Hi-Z
SDCLK	B6	O	L	#RTS1	R7	O	Hi-Z
#SDCD	C7	I	-	RXD1	R8	I	Hi-Z
SDWP	B7	I	-	#CTS1	R9	I	-

***** This signal is not controlled by #SUSPEND signal. The state before suspend mode (#SUSPEND=low) is held.

NAME	Pin	IO	State	NAME	Pin	IO	State
RRXD	L1	O	H	XST	H1	O	L
#RCTS	L2	O	H	NXST	J1	O	L
#RDCD	M2	O	L	YCK	K1	O	L
#RDSR	N1	O	H	NYCK	E2	O	L
#RRI	N2	O	H	YST	F2	O	L
RVON	R10	O	H	NYST	G2	O	L
RTXD	P1	I	Hi-Z	COM	H2	O	L
#RRTS	P2	I	Hi-Z	PREC	J2	O	L
#RDTR	P3	I	Hi-Z	#PREC	K2	O	L
#CONT2	P10	O	Hi-Z	PPOL	E3	O	L
#CONT1	R11	O	Hi-Z	#PPOL	F3	O	L
#DTR1	P11	O	Hi-Z	LHSYNC	G3	I	-
#PUPD	P12	O	Hi-Z	LVSYNC	H3	I	-
#DSR1	R13	I	Hi-Z	LDE	J3	I	-
#DET1	P13	I	Hi-Z	LSCLK	K3	I	-
SEL1	P14	I	H	HCLK	B12	I	-
SEL0	R14	I	H	CK48M	A12	I	-
#P1CD	C13	O	-	CLK32	B10	I	-
#P2CD	K4	O	-	#HINT	A14	O(OD)	Hi-Z
#PWAIT	D13	O	-	#PCLR	A10	I	-
#PIO16	D12	O	-	#SUSPEND	A9	I	-
#S1COE	C12	O	-	DISEL1	B9	I	-
#S2COE	L5	O	-	DISEL0	A11	I	-
#DIR	D6	O	-	SRSEL	C8	I	-
#S1DOE	D11	O	-	LVSEL	C9	I	-
#S2DOE	L4	O	-	DMDAT	C10	O	-
#S1CD2	D9	I	H	L3VON	C11	I	-
#S1CD1	D10	I	H	TST0	F4	I	-
#S2CD2	M3	I	H	TST1	G4	I	-
#S2CD1	L3	I	H	TST2	H4	I	-
#S1WAIT	D8	I	H	TST3	J4	I	-
#S2WAIT	M4	I	H	#RSV0	A13	O(OD)	Hi-Z
#S1IOIS16	D7	I	H	RSV0	B11	I	-
#S2IOIS16	M5	I	H	RSV1	B8	I	-
#PCE2	C14	I	-	RSV2	B13	I	-
#PCE1	C15	I	-				
#POE	B15	I	-				
#PIOR	B14	I	-				
PSKTSEL	E12	I	-				
CPH	D1	O	L				
STH	E1	O	L				
XCK	F1	O	L				
NXCK	G1	O	L				

***** This signal is not controlled by #SUSPEND signal. The state before suspend mode (#SUSPEND=low) is held.

4.11 Pull-up/down Resistance

PULL- UP/DOWN resistance is to be installed for each interface in TC6391XB. Be aware that resistance values (described "Res. Val." in the following tables) indicated in the following tables are provided only for references.

4.11.1 Host Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
HRDY	E11	O (OD)	Pull-up	VDD	10KΩ	Ready

4.11.2 SD Card Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
SDCD3	A5	IO	Pull-up	SDVDD	10-100KΩ	SD Card Slot / Data Bus
SDCD2	A6		Pull-up	SDVDD	10-100KΩ	
SDCD1	A7		Pull-up	SDVDD	10-100KΩ	
SDCD0	A8		Pull-up	SDVDD	10-100KΩ	
SDCMD	B5	IO	Pull-up	SDVDD	10-100KΩ	SD Card Slot /Command
SDCLK	B6	O	-	-	-	SD Card Slot / Clock
#SDCD	C7	I	-	-	-	SD Card Slot / Detection
SDWP	B7	I	-	-	-	SD Card Slot / Write Protection
SDLED	C5	O	-	-	-	SD Card Slot / SDLED signal

4.11.3 SmartMedia™ Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
SMD7	P4	IO	-	-	-	Data 7-0
SMD6	P5					
SMD5	P6					
SMD4	P7					
SMD3	P8					
SMD2	P9					
SMD1	N9					
SMD0	N10					
SMCLE	N3	O (3state)	Pull-down	-	100KΩ	Command Latch Enabled
SMALE	N4	O (3state)	Pull-down	-	100KΩ	Address Latch Enabled
#SMWE	N5	O (3state)	Pull-up	SMVDD	100KΩ	Write Enabled
#SMRE	N6	O (3state)	Pull-up	SMVDD	100KΩ	Read Enabled
#SMCE	N7	O (3state)	Pull-up	SMVDD	100KΩ	Chip Enabled
#SMWP	N8	O (3state)	Pull-down	-	100KΩ	Write Protection
#SMRB	M10	I	Pull-up	SMVDD	10KΩ	Busy
#SMCD	M11	I	-	-	-	Low-Voltage Detection
SMLVD	M12	I	-	-	-	Card Detection
#SMWPD	N11	I	-	-	-	Write Protection Seal
#SMEJSW	N12	I	-	-	-	Ejection Request
#SMLED	M6	O (OD)	Pull-up	VDD	100KΩ	LED ON
#SMLOCK	M7	O (OD)	Pull-up	VDD	100KΩ	Lock Mode
#SMEJCT	M8	O (OD)	Pull-up	VDD	100KΩ	Ejection Response

4.11.4 USB Host Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
USB1DP	B3	IO	Pull-down	-	15KΩ	USB Port 1 Data+
USB1DN	A2		Pull-down	-	15KΩ	USB Port 1 Data-
USB2DP	C3		Pull-down	-	15KΩ	USB Port 2 Data+
USB2DN	B1		Pull-down	-	15KΩ	USB Port 2 Data-
USB3DP	C1		Pull-down	-	15KΩ	USB Port 3 Data+
USB3DN	D2		Pull-down	-	15KΩ	USB Port 3 Data-
PPON1	B4	O	-	-	-	USB Port 1/Power Supply Control
PPON2	C4	O	-	-	-	USB Port 2/Power Supply Control
PPON3	D5	O	-	-	-	USB Port 3/Power Supply Control
#USBOC	A3	I	Pull-up	VDD	10KΩ	USB Over Current

4.11.5 Serial Port Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
TXD0	R2	O	Pull-up	VDD	47KΩ	Synchronous Send Data
RXD0	R3	I	-	-	-	Synchronous Receive Data
FRM0	R4	I	-	-	-	Frame Clock
SCK0	R5	I	-	-	-	Serial Clock
TXD1	R6	O	Pull-up	VDD	47KΩ	Asynchronous Send Data
#RTS1	R7	O	Pull-up	VDD	47KΩ	Request to Send
RXD1	R8	I	-	-	-	Asynchronous Receive Data
#CTS1	R9	I	-	-	-	Clear to Send
RRXD	L1	O	-	-	-	Asynchronous Receive Data to Host
#RCTS	L2	O	-	-	-	Clear to Send to Host
#RDCD	M2	O	-	-	-	Data Carrier Detect to Host
#RDSR	N1	O	-	-	-	Data Set Ready to Host
#RRI	N2	O	-	-	-	Ring Indicate to Host
RVON	R10	O	-	-	-	Power Switch select to Driver/Receiver
RTXD	P1	I	-	-	-	Asynchronous Send Data from Host
#RRTS	P2	I	-	-	-	Request to Send from Host
#RDTR	P3	I	-	-	-	Data Terminal Ready from Host
#CONT2	P10	O	Pull-up	VDD	47KΩ	Serial Port control
#CONT1	R11	O	Pull-up	VDD	47KΩ	Serial Port control
#DTR1	P11	O	Pull-up	VDD	47KΩ	Data Terminal Ready to
#PUPD	P12	O	Pull-up	VDD	10KΩ	Pull-up/Pull-down control
#DSR1	R13	I	-	-	-	Data set Ready from
#DET1	P13	I	-	-	-	Device detect
SEL1	P14	I	-	-	-	External Device select
SEL0	R14	I	-	-	-	External Device select

4.11.6 CompactFlash Control Interface

CompactFlash Control interface does not need external resistances.

4.11.7 Low Polysilicon TFT-LCD Converter Control Interface

Low Polysilicon TFT-LCD Converter Control interface does not need external resistances.

4.11.8 System Interface

NAME	Pin	IO	Pull-up/ Pull-down	Pull-up Power	Res. Val.	FUNCTION/REMARKS
#HINT	A14	O (OD)	Pull-up	VDD	10KΩ	Interruption

4.12 Processing Unused InterfaceExternal Pins

TC6391XB equips with any interfaces of SD Card, SmartMedia™, USB host Serial port, CompactFlash control and Low Polysilicon TFT-LCD Converter control. See descriptions for processing pins in respective sections of interface when dealing with unused External Pins for interfaces.

4.12.1 Processing Pins (SmartMedia™ Interface unsupported)

Process Pins according to the following table when SmartMedia™ Interface is unused (when each signals are not connected to other parts) :

NAME	Pin	I/O	Process
SMD7	P4	IO	Open
SMD6	P5	IO	Open
SMD5	P6	IO	Open
SMD4	P7	IO	Open
SMD3	P8	IO	Open
SMD2	P9	IO	Open
SMD1	N9	IO	Open
SMD0	N10	IO	Open
SMCLE	N3	O(3state)	Open
SMALE	N4	O(3state)	Open
#SMWE	N5	O(3state)	Open
#SMRE	N6	O(3state)	Open
#SMCE	N7	O(3state)	Open
#SMWP	N8	O(3state)	Open
#SMRB	M10	I	Fixed to direct High.
SMLVD	M11	I	Open
#SMCD	M12	I	Open
#SMWPD	N11	I	Open
#SMEJSW	N12	I	Open
#SMLED	M6	O(OD)	Open
#SMLOCK	M7	O(OD)	Open
#SMEJCT	M8	O(OD)	Open
SMVC3EN	M9	O	Open

4.12.2 Processing Pins (SD Interface unsupported)

Process Pins according to the following table when SD Interface is unused (when each signals are not connected to other parts):

NAME	Pin	I/O	Process
SDCD3	A5	IO	Fixed to direct GND.
SDCD2	A6	IO	Fixed to direct GND.
SDCD1	A7	IO	Fixed to direct GND.
SDCD0	A8	IO	Fixed to direct GND.
SDCMD	B5	IO	Fixed to direct GND.
SDCLK	B6	O	Open
#SDCD	C7	I	Open
SDWP	B7	I	Open
SDLED	C5	O	Open
SDPWR	C6	O	Open

4.12.3 Processing Pins (USB Host Interface unsupported)

Process pins according to the following figure when USB Host Interface is unused (when each signals are not connected to other parts):

NAME	Pin	I/O	Process
USB1DP	B3	IO	Fixed to direct GND.
USB1DN	A2	IO	Fixed to direct GND.
USB2DP	C3	IO	Fixed to direct GND.
USB2DN	B1	IO	Fixed to direct GND.
USB3DP	C1	IO	Fixed to direct GND.
USB3DN	D2	IO	Fixed to direct GND.
PPON1	B4	O	Open
PPON2	C4	O	Open
PPON3	D5	O	Open
#USBOC	A3	I	Fixed to direct High.

4.12.4 Processing Pins (Serial Port Interface unsupported)

Process pins according to the following figure when Serial Port Interface is unused (when each signals are not connected to other parts):

NAME	Pin	I/O	Process
TXD0	R2	O	Open
RXD0	R3	I	Fixed to direct GND.
FRM0	R4	I	Fixed to direct GND.
SCK0	R5	I	Fixed to direct GND.
TXD1	R6	O	Open
#RTS1	R7	O	Open
RXD1	R8	I	Fixed to direct GND.
#CTS1	R9	I	Fixed to direct High.
RRXD	L1	O	Open
#RCTS	L2	O	Open
#RDCD	M2	O	Open
#RDSR	N1	O	Open
#RRI	N2	O	Open
RVON	R10	O	Open
RTXD	P1	I	Fixed to direct GND.
#RRTS	P2	I	Fixed to direct High.
#RDTR	P3	I	Fixed to direct High.
#CONT2	P10	O	Open
#CONT1	R11	O	Open
#DTR1	P11	O	Open
#PUPD	P12	O	Open
#DSR1	R13	I	Fixed to direct High.
#DET1	P13	I	Fixed to direct High.
SEL1	P14	I	Open
SEL0	R14	I	Open

4.12.5 Processing Pins (CompactFlash Control Interface unsupported)

Process pins according to the following figure when CompactFlash Control Interface is unused (when each signals are not connected to other parts):

NAME	Pin	I/O	Process
#P1CD	C13	O	Open
#P2CD	K4	O	Open
#PWAIT	D13	O	Open
#PIO16	D12	O	Open
#S1COE	C12	O	Open
#S2COE	L5	O	Open
#DIR	D6	O	Open
#S1DOE	D11	O	Open
#S2DOE	L4	O	Open
#S1CD2	D9	I	Open
#S1CD1	D10	I	Open
#S2CD2	M3	I	Open
#S2CD1	L3	I	Open
#S1WAIT	D8	I	Open
#S2WAIT	M4	I	Open
#S1IOIS16	D7	I	Open
#S2IOIS16	M5	I	Open
#PCE2	C14	I	Fixed to direct High.
#PCE1	C15	I	Fixed to direct High.
#POE	B15	I	Fixed to direct High.
#PIOR	B14	I	Fixed to direct High.
PSKTSEL	E12	I	Fixed to direct GND.

4.12.6 Processing Pins (Low Polysilicon TFT-LCD Converter Control Interface unsupported)

Process pins according to the following figure when Low Polysilicon TFT-LCD Converter Control Interface is unused (when each signals are not connected to other parts):

NAME	Pin	I/O	Process
CPH	D1	O	Open
STH	E1	O	Open
XCK	F1	O	Open
NXCK	G1	O	Open
XST	H1	O	Open
NXST	J1	O	Open
YCK	K1	O	Open
NYCK	E2	O	Open
YST	F2	O	Open
NYST	G2	O	Open
COM	H2	O	Open
PREC	J2	O	Open
#PREC	K2	O	Open
PPOL	E3	O	Open
#PPOL	F3	O	Open
LHSYNC	G3	I	Fixed to direct GND.
LVSYNC	H3	I	Fixed to direct GND.
LDE	J3	I	Fixed to direct GND.
LSCLK	K3	I	Fixed to direct GND.

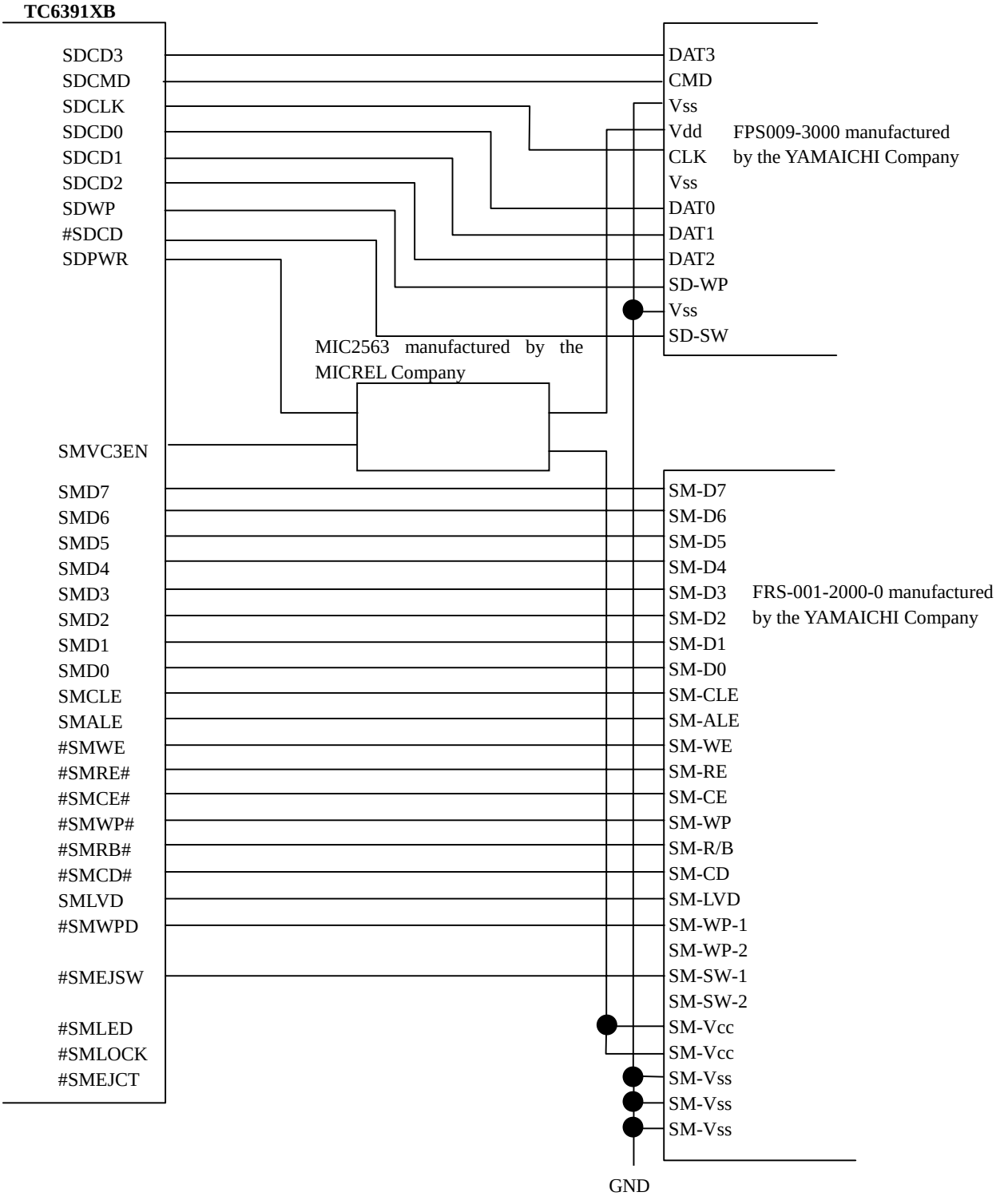
4.12.7 Processing Pins for Signals unused in System Interface

Process Pins according to the following table when Signals are unused (when each signals are not connected to other parts) in System Interface listed below:

NAME	Pin	I/O	Process
#HINT	A14	O(OD)	Open
#SUSPEND	A9	I	Fixed to direct High.
DMDAT	C10	O	Open
L3VON	C11	I	Fixed to direct GND.

4.13 Connection example of SD Card/SmartMedia™ socket

It is shown that total 32 signal connections example of TC6391XB which have 8 signals of SD card interface(except SDLED signal), 1 signal of a power supply control for SD card, 22 signals of SmartMedia™ interface and 1 signal of a power supply control for SmartMedia™. An outside pull-up/down resistance that is mentioned on an item of the "4.12 Pull-up/down resistance" is not shown in a bottom figure. When you design a circuit, please refer to recommended resistance by an item of the "4.12 Pull-up/down " and a bottom figure.



4.14 GPIO interface specification

SmartMedia interface signals can be used as GPIO interface signals by setting DISEL[1:0] signals to 10b.

NAME	Pin	IO	Power Supply	While SmartMedia I/F
GPI12	M10	I	VDD	#SMRB
GPI11	M11	I		#SMCD
GPI10	M12	I		SMLVD
GPI9	N11	I		#SMWPD
GPI8	N12	I		#SMEJSW
GPI7	P4	IO		SMD7
GPI6	P5	IO		SMD6
GPI5	P6	IO		SMD5
GPI4	P7	IO		SMD4
GPI3	P8	IO		SMD3
GPI2	P9	IO		SMD2
GPI1	N9	IO		SMD1
GPI0	N10	IO		SMD0
GPO6	M9	O		SMVC3EN
GPO5	N3	O (3state)		SMCLE
GPO4	N4	O (3state)		SMALE
GPO3	N5	O (3state)		#SMWE
GPO2	N6	O (3state)		#SMRE
GPO1	N7	O (3state)		#SMCE
GPO0	N8	O (3state)		#SMWP

4.14.1 GPI[12:0] signals

The status of GPI[12:0] signals can be read by GPI Status Register(Config Offset: F2h) in System Configuration Register.

<GPI Status Register>

Config	RW	D15	D14	D13	D12	D11	D10	D9	D8	#PCLR
F2h	R	-	-	-	GPI12	GPI11	GPI10	GPI9	GPI8	-
		D7	D6	D5	D4	D3	D2	D1	D0	
		GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0	

4.14.2 GPO[6:0] signals

GPO[6:0] signals can be switched to output mode by writing 0b to each bits of GPO Output Enable Register(Config Offset: F1h) in System Configuration Register. The values written to GPO Output Control Register(Config Offset: F0h) are output to GPO[6:0] signals.

<GPO Output Enable Register>

Config	RW	D7	D6	D5	D4	D3	D2	D1	D0	#PCLR
F1h	RW	-	ENGPO6	ENGPO5	ENGPO4	ENGPO3	ENGPO2	ENGPO1	ENGPO0	7Fh

<GPO Output Control Register>

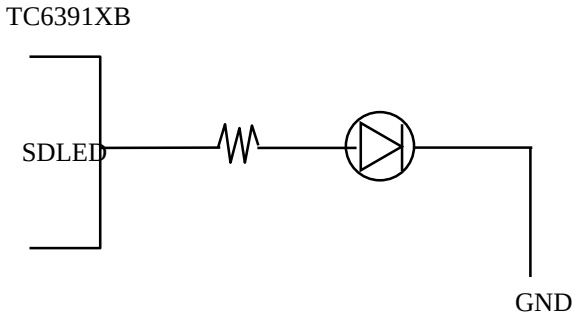
Config	RW	D7	D6	D5	D4	D3	D2	D1	D0	#PCLR
F0h	RW	-	CTGPO6	CTGPO5	CTGPO4	CTGPO3	CTGPO2	CTGPO1	CTGPO0	00h

4.15 SDLED/#SMLED signal

4.15.1 SDLED signal

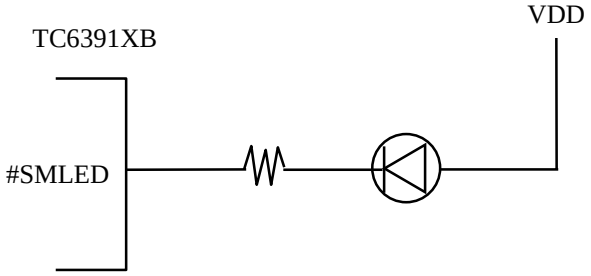
TC6391XB has the SDLED signal for SD interface. This signal is controlled by setting SDLED Control Register(Offset:13Eh). Before accessing SDLED Control Register(Offset:13Eh), please set following registers.

*Set SDLED Enable Register 1(Config Offset:FAh) to 12h.
*Set SDLED Enable Register 2(Config Offset:FEh) to 80h.



4.15.2 #SMLED signal

TC6391XB has the #SMLED signal for SmartMedia™ interface. This signal is controlled by setting Mode Register(Offset:04h) of SmartMedia™ control register. When Mode Register is written 04h, #SMLED becomes low and LED turns on. In reverse, in the case of being written 00h, #SMLED becomes high and LED turns off.



5. Electrical Characteristics

5.1 Absolute Maximum Standard

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition	Note
VDD	Supply Voltage Range	-0.3	5.0	V	GND=0V	1
Vin3	Input Voltage (3.3V)	-0.3	VDD+0.3	V	GND=0V	
Vout	Output Voltage	-0.3	VDD+0.3	V	GND=0V	
Tstg	Storage Temperature Range	-40	125	degree C		

Note 1: VDD Power Supply

Note: Absolute Maximum Ratings indicates that stress greater than the values described above might cause permanent damages to the devices and does not guarantee all the performances within Absolute Maximum Ratings

5.2 DC Characteristic

5.2.1 Recommended Conditions for proper performances

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD	Supply Voltage for Core Logic	3.0	3.3	3.6	V	
VDDS	Supply Voltage for I/O	2.3		3.6		
Topr	Ambient Temperature under bias				degree C	**T.B.D**

5.2.2 Host Interface DC Characteristic

Host Interface DC Characteristic(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage			V		1-1
Vil	Input Low Voltage			V		1-1
Iilk	Input Leakage Current			uA		1-1
Voh	Output High Voltage			V		1-2
Vol	Output Low Voltage			V		1-2

T.B.D

Note1-1: Applied for HD[15-0] ,HA[13-1], #HCS, #HOE, #HWE, #HBEL, #HBEH pins

Note1-2: Applied for HD[15-0], HRDY pins

5.2.3 SmartMedia™ Interface DC Characteristic

SmartMedia™ Interface DC Characteristic: 3.3V Operation
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage			V		2-1
Vil	Input Low Voltage			V		2-1
Voh	Output High Voltage			V		2-2
Vol1	Output Low Voltage			V		2-2
Vol2	Output Low Voltage			V		2-3
Iilk	Input Leakage Current			uA		2-1

Note2-1 Applied for SMD[7:0], #SMRB, #SMCD, SMLVD, #SMWPD, #SMEJSW pins

Note2-2 Applied for SMD[7:0], SMCLE, SMALE, #SMCE, #SMWE, #SMRE, #SMWP pins

Note2-3 Applied for #SMLOCK, #SMEJCT, #SMLED pins

5.2.4 SmartMedia™ Power Supply Control DC Characteristic

SmartMedia™ Power Supply Control DC Characteristic: 3.3V Operation
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Voh	Output High Voltage			V		2-3
Vol	Output Low Voltage			V		2-3

Note2-3 Applied for SMVC3EN pin

5.2.5 SD Card Interface Pin DC Characteristic

SD Card Interface DC Characteristic: 3.3V Operation
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage			V		3-1
Vil	Input Low Voltage			V		3-1
Vih	Input High Voltage			V		3-2
Vil	Input Low Voltage			V		3-2
Voh	Output High Voltage			V		3-3
Vol	Output Low Voltage			V		3-3
Iilk	Input Leakage Current			uA		3-1 3-2
Rdat3	Pull-up resistance inside card (pin1)			KΩ		

Note3-1 Applied for SDCD[3:0], SDCMD, SDWP pins

Note3-2 Applied for #SDCD pin

Note3-3 Applied for SDCD[3:0], SDCMD, SDCLK, SDLED pins

5.2.6 SD Card Power Supply Control DC Characteristic

SD Card Power Supply Control DC Characteristic: 3.3V Operation
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Voh	Output High Voltage			V		3-4
Vol	Output Low Voltage			V		3-4

Note3-4 Applied for SDPWR pin

5.2.7 USB Host Interface Pin DC Characteristic

USB Host Interface Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage			V		4-1
Vil	Input Low Voltage			V		4-1
Iilk	Input Leakage Current			uA		4-1
Voh	Output High Voltage			V		4-2
Vol	Output Low Voltage			V		4-2

T.B.D

Note4-1 Applied for USB1DP, USB1DN, USB2DP, USB2DN, USB3DP, USB3DN, #USBOC pins

Note4-2 Applied for USB1DP, USB1DN, USB2DP, USB2DN, USB3DP, USB3DN pins

5.2.8 USB Port Power Supply Control DC Characteristic

USB Port Power Supply Control DC Characteristic: 3.3V Operation
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Voh	Output High Voltage			V		4-3
Vol	Output Low Voltage			V		4-3

T.B.D

Note4-3 Applied for PPON1, PPON2, PPON3 pins

5.2.9 Serial Host Interface Pin DC Characteristic

Serial Host Interface Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage			V		5-1
Vil	Input Low Voltage			V		5-1
Iilk	Input Leakage Current			uA		5-1
Voh	Output High Voltage			V		5-2
Vol	Output Low Voltage			V		5-2

T.B.D

Note5-1 Applied for RXD0, FRM0, SCK0, RXD0, #CTS1, RTXD, #RRTS, #RDTR, #DSR1, #DET1, SEL1, SEL0 pins

Note5-2 Applied for TXD0, TXD1, #RTS1, RRXD, #RCTS, #RDCD, #RDSR, #RRI, RVON, #CONT2, #CONT1, #DTR1 pins

5.2.10 CompactFlash Control Interface Pin DC Characteristic

CompactFlash Control Interface Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage			V		6-1
Vil	Input Low Voltage			V		6-1
Iilk	Input Leakage Current			uA		6-1
Voh	Output High Voltage			V		6-2
Vol	Output Low Voltage			V		6-2

T.B.D

Note6-1 Applied for #S1CD2, #S1CD1, #S2CD2, #S2CD1, #S1WAIT, #S2WAIT, #S1IOIS16, #S2IOIS16, #PCE2, #PCE1, #POE, #PIOR, PSKTSEL pins

Note6-2 Applied for #P1CD, #P2CD, #PWAIT, #PIO16, #S1COE, #S2COE, #DIR, #S1DOE, #S2DOE pins

5.2.11 Low Polysilicon TFT-LCD Converter Control Interface Pin DC Characteristic

Low Polysilicon TFT-LCD Converter Control Interface Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage			V		7-1
Vil	Input Low Voltage			V		7-1
Iilk	Input Leakage Current			uA		7-1
Voh	Output High Voltage			V		7-2
Vol	Output Low Voltage			V		7-2

T.B.D

Note7-1 Applied for LHSYNC, LVSYNC, LDE, LSCLK pins

Note7-2 Applied for CPH, STH, XCK, NXCK, XST, NXST, YCK, NYCK, YST, NYST, COM, PREC, #PREC, PPOL, #PPOL pins

5.2.12 System Interface Pin DC Characteristic

System Interface Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
Vih	Input High Voltage			V		8-1
Vil	Input Low Voltage			V		8-1
Iilk	Input Leakage Current			uA		8-1
Voh	Output High Voltage			V		8-2
Vol	Output Low Voltage			V		8-2

T.B.D

Note8-1 Applied for HCLK, CK48M, CLK32, #PCLR, #SUSPEND, DISEL[1-0] , SRSEL, LVSEL, L3VON pins

Note8-2 Applied for #HINT, DMDAT pins

5.2.13 TEST Pin DC Characteristic

TEST Pin DC Characteristic
(VDD = V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Condition	Note
Vih	Input High Voltage			V		9-1
Vil	Input Low Voltage			V		9-1
Iilk	Input Leakage Current			μA		9-1

T.B.D

Note9-1 Applied for TST[3:0] pins

5.2.14 Power Consumption Characteristic

Power Supply Current

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Iccstd1	Power Supply Current, Standby				uA	HCLK=0, CLK32=0 VDD=3.6V #SUSPEND=low
Iccstd2	Power Supply Current, Standby				uA	HCLK=0, CLK32=32KHz VDD=3.6V #SUSPEND=low
IccSM	Power Supply Current, Operating SmartMedia™				mA	HCLK=33MHz, CLK32=32KHz VDD=3.6V
IccSD/MMC	Power Supply Current, Operating SD Card or MultiMedia Card				mA	HCLK=33MHz, CLK32=32KHz VDD=3.6V

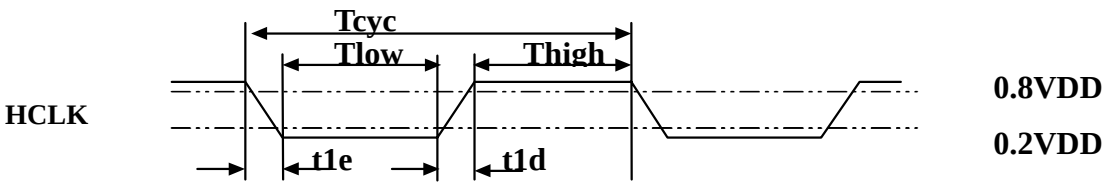
5.3 AC Characteristic

5.3.1 Host Interface Signal AC Characteristic

(1)System Clock AC Characteristic
(VDD= V, Ta= degree C)

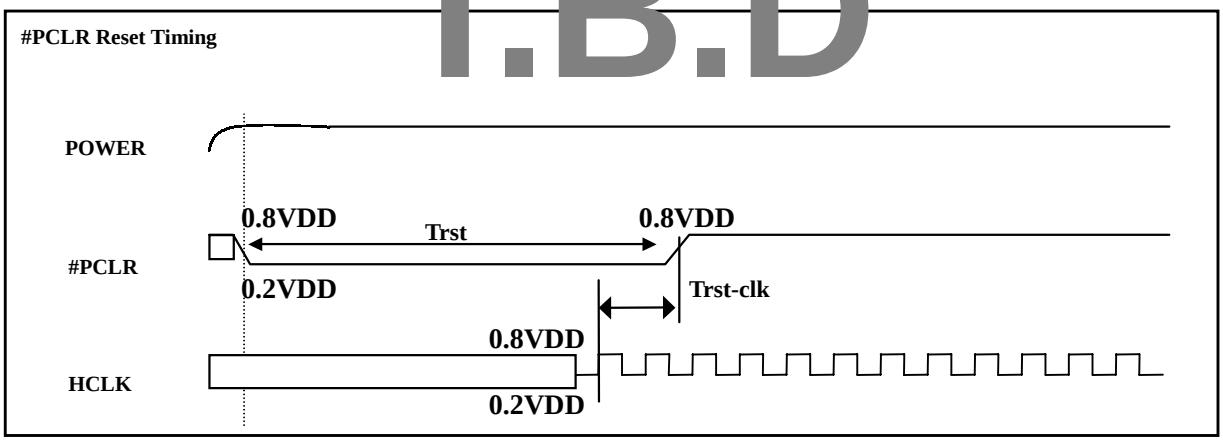
Symbol	Parameter	Min	Max	Unit	Notes
	HCLK				
Tcyc	CLK cycle time			ns	
Thigh	CLK High time			ns	
Tlow	CLK Low time			ns	
t1d	HCLK Rising Time			ns	
t1e	HCLK Falling Time			ns	

HCLK Timing



(2)#PCLR Reset AC Characteristic
(VDD= V, Ta= degree C)

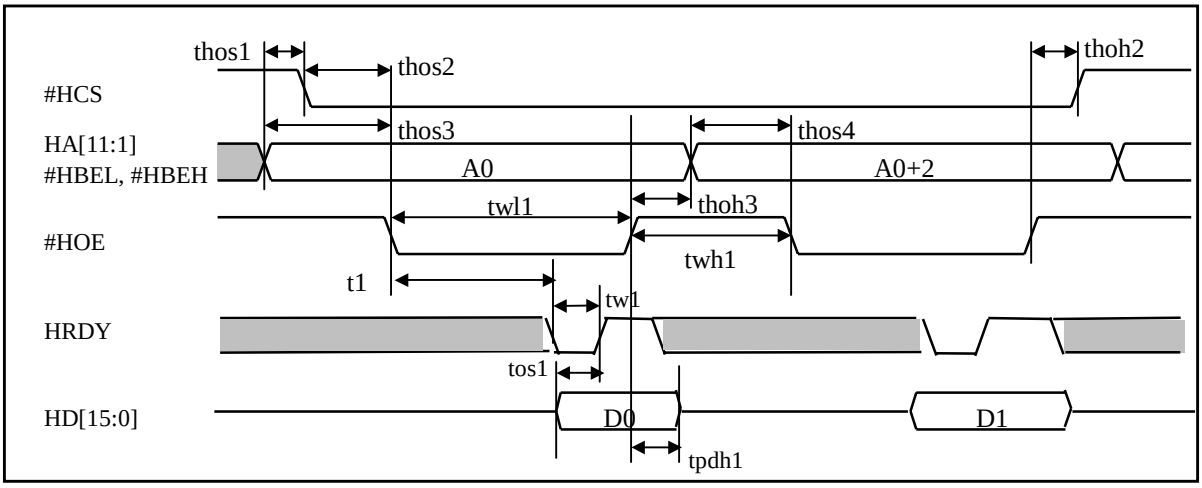
Symbol	Parameter	Min	Max	Unit	Notes
	#PCLR				
Trst	Reset active time after power stable			ms	
Trst-clk	Reset active time after CLK stable			ms	

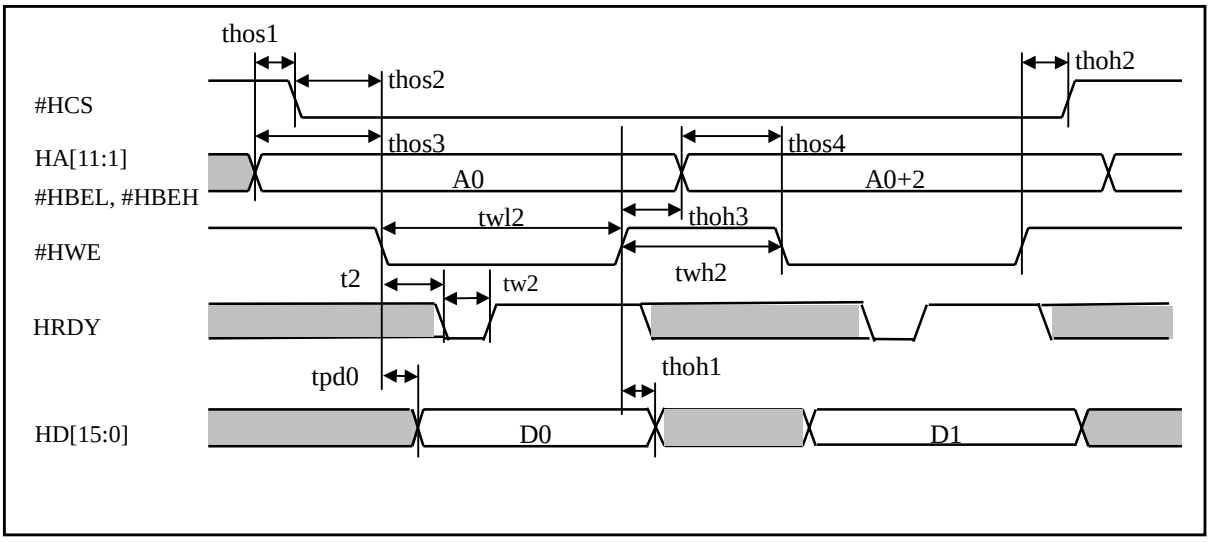


#PCLR Reset Timing

(3)Standard Memory Interface Signal AC Characteristic
(VDD= V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Notes
thos1	Address setup to #HCS			ns	
thos2	#HCS, #HBEL, #HBEH setup to #HOE or #HWE			ns	
thos3	Address setup to #HOE or #HWE low			ns	
thos4	Address setup to #HOE or #HWE low			ns	
tpd0	Data delay time after #HWE low			ns	
thoh1	Data hold after #HWE high			ns	
thoh2	#HCS, #HBEL, #HBEH hold after #HOE or #HWE de-assert			ns	
thoh3	Address Hold after #HCS or #HWE de-asserted			ns	
twh1	#HOE high time			ns	
twh2	#HWE high time			ns	
twl1	#HOE low time			ns	
twl2	#HWE low time			ns	
tos1	Data Setup for HRDY Release			ns	
tpdh1	#HOE,HD[15:0] hold time			ns	
t1	#HOE low to HRDY low time			ns	
t2	#HWE low to HRDY low time			ns	
tw1	HRDY low time			ns	
tw2	HRDY low time			ns	


thos1
thos2
thoh2
#HCS
HA[11:1]
#HBEL, #HBEH
thos3
thos4
A0
A0+2
twl1
thoh3
#HOE
twh1
t1
tw1
HRDY
tos1
HD[15:0]
D0
D1
tpdh1


thos1
thos2
thoh2
#HCS
HA[11:1]
#HBEL, #HBEH
thos3
thos4
A0
A0+2
twl2
thoh3
#HWE
t2
tw2
twh2
HRDY
tpd0
thoh1
HD[15:0]
D0
D1

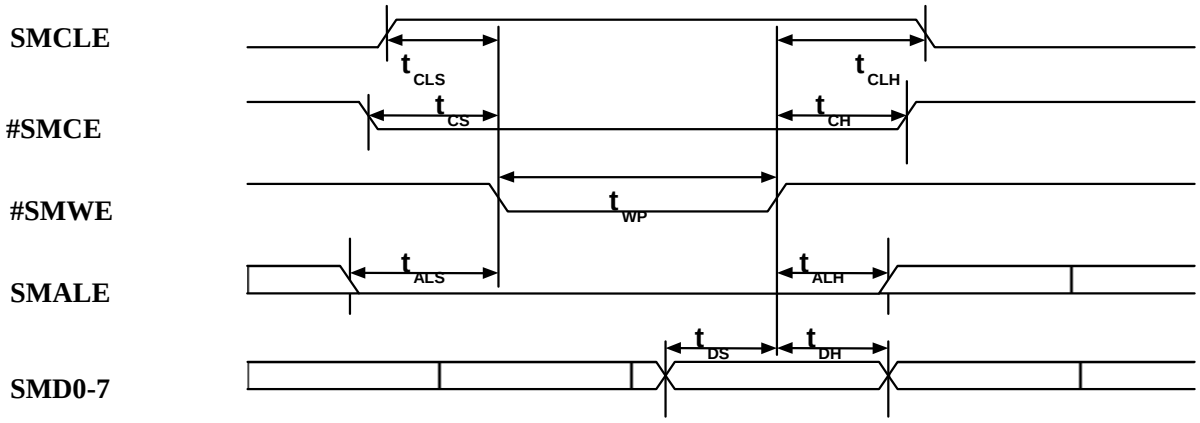
5.3.2 SmartMedia™ Interface Signal AC Characteristic
(VDD= V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit
t_{CLS}	SMCLE Setup Time			ns
t_{CLH}	SMCLE Hold Time			ns
t_{CS}	#SMCE Setup Time			ns
t_{CH}	#SMCE Hold Time			ns
t_{WP}	#SMWE Pulse Width			ns
t_{ALS}	SMALE Setup Time			ns
t_{ALH}	SMALE Hold Time			ns
t_{DS}	Data Setup Time			ns
t_{DH}	Data Hold Time			ns
t_{WH}	#SMWE High Hold Time			ns
t_{WW}	#SMWP High to #SMWE Low			ns
t_{RR}	Ready to #SMRE Low			ns
t_{RP}	Read Pulse Width			ns
t_{RC}	Read Cycle Time			ns
t_{CEH}	#SMCE High Hold Time(at the Last Serial Read)			ns
t_{REH}	#SMRE High Hold Time			ns
t_{IR}	Output Hi-Z to #SMRE Low			ns
t_{WHC}	#SMWE High to #SMCE Low			ns
t_{WHR}	#SMWE High to #SMRE Low			ns
t_{AR1}	SMALE Low to #SMRE Low (Address Register Read, ID Read)			ns
t_{CR}	#SMCE Low to #SMRE Low (Data Register Read ,ID Read)			ns

AC Test Conditions

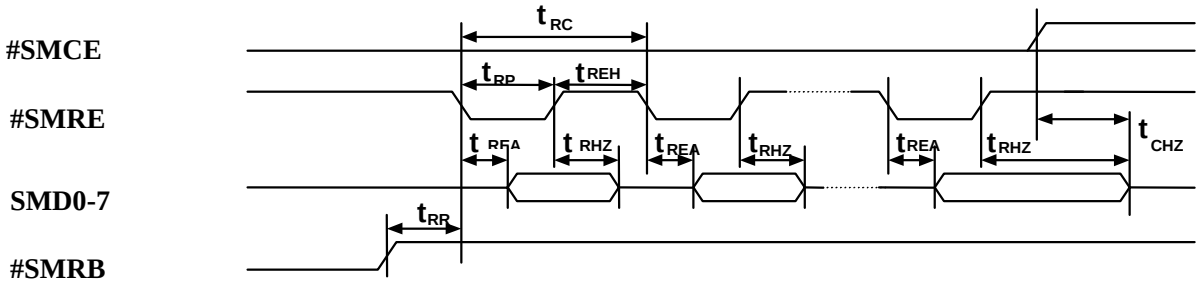
Parameter	3.3V Model
Input Pulse Level	
Input comparison Level	
Output Data comparison Level	
Output Load	

Command Cycle Timing



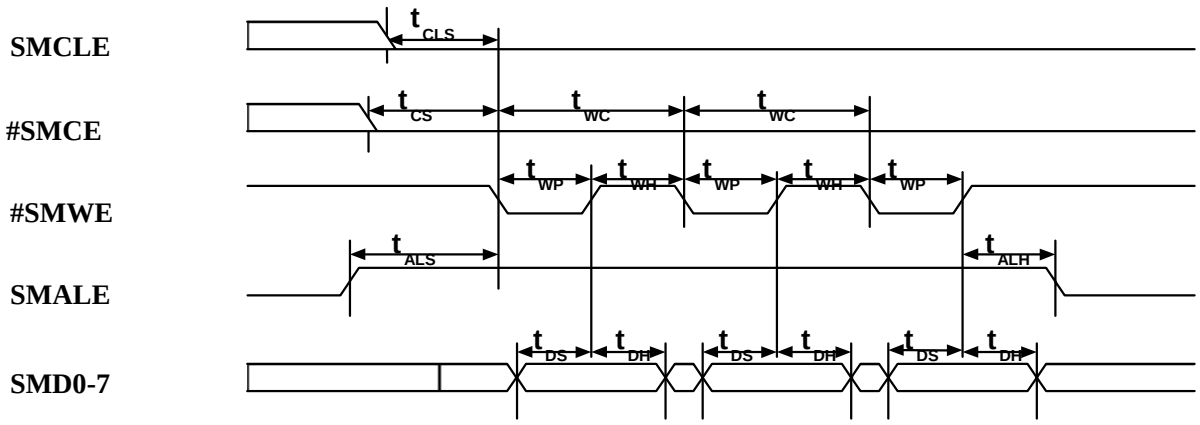
Timing for Command Cycle Signals

Serial Read Cycle Timing



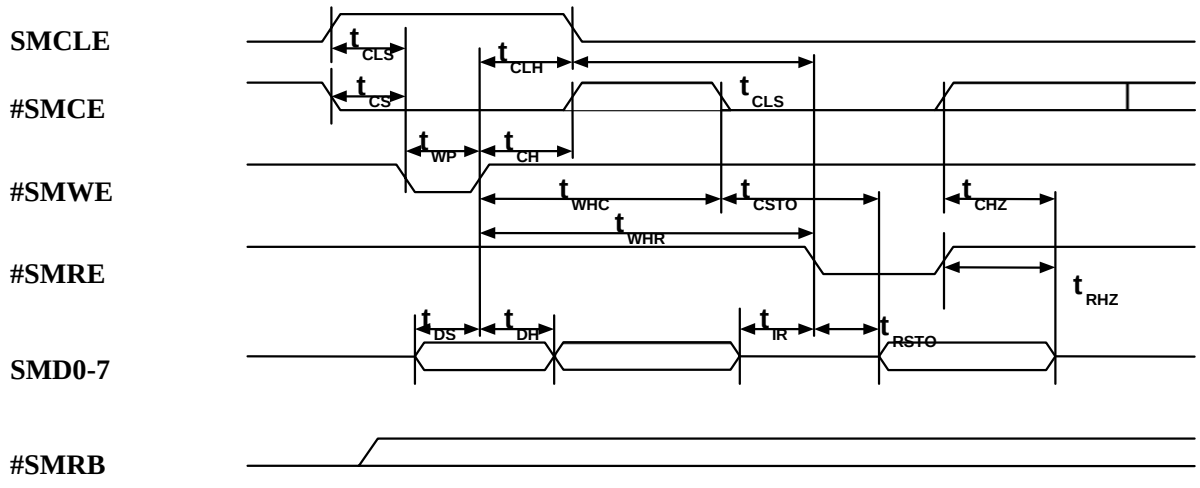
Timing for Serial Read Cycle Signals

Address Cycle Timing



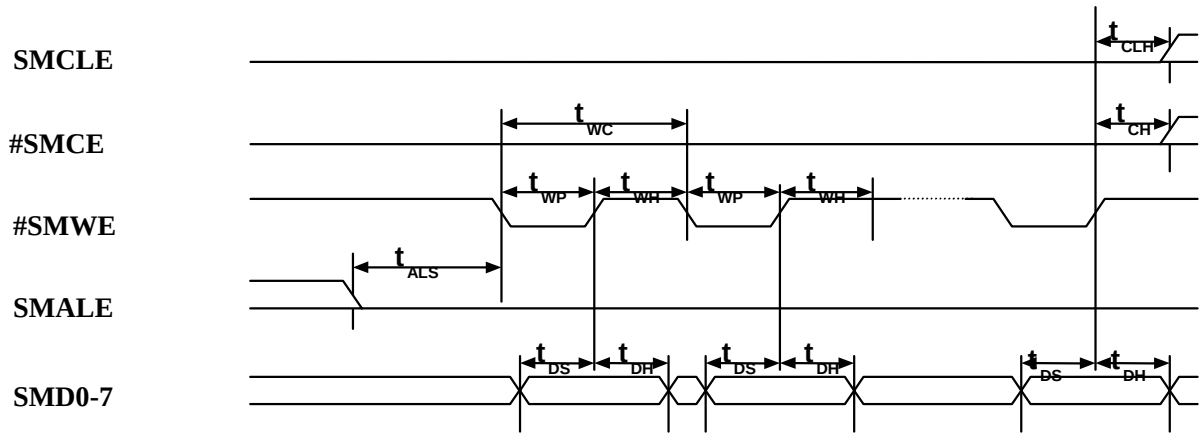
Timing for Address Cycle Signals

Status Read Cycle Timing



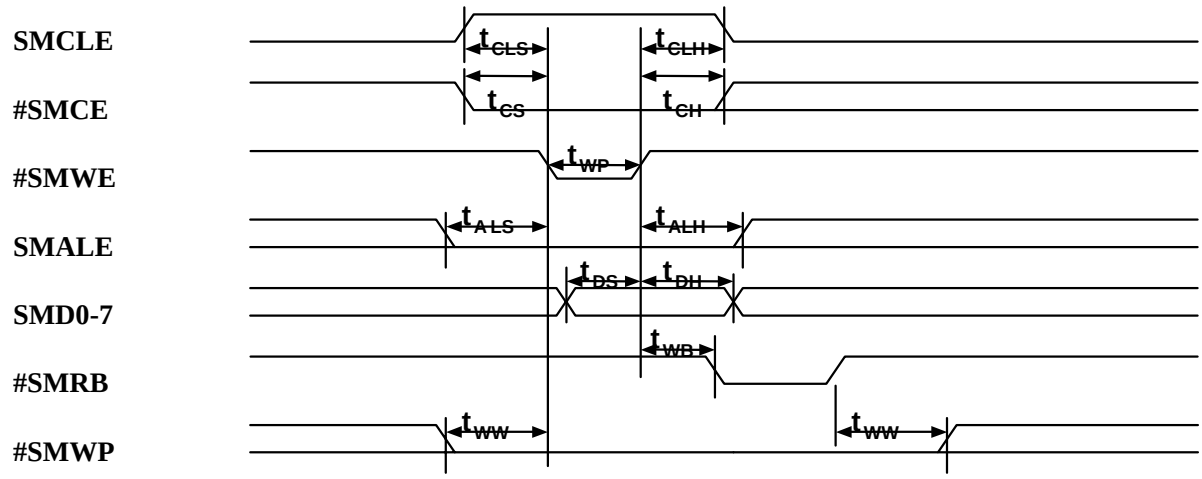
Timing for Status Read Cycle Signals

Data Write Cycle Timing



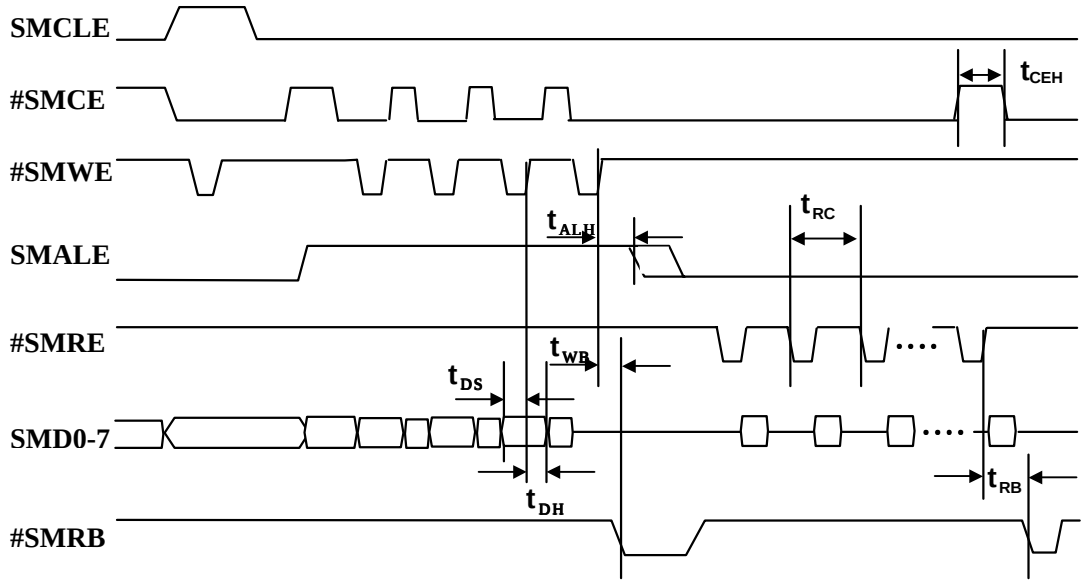
Timing for Data Write Cycle Signals

Reset Cycle Timing



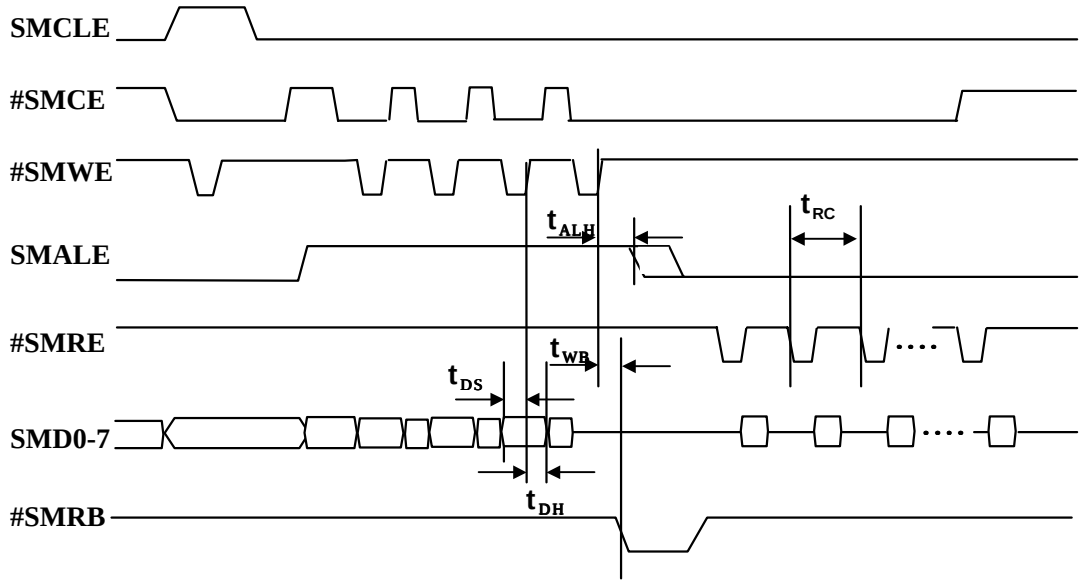
Timing for Reset Cycle Signals

Read Cycle Timing



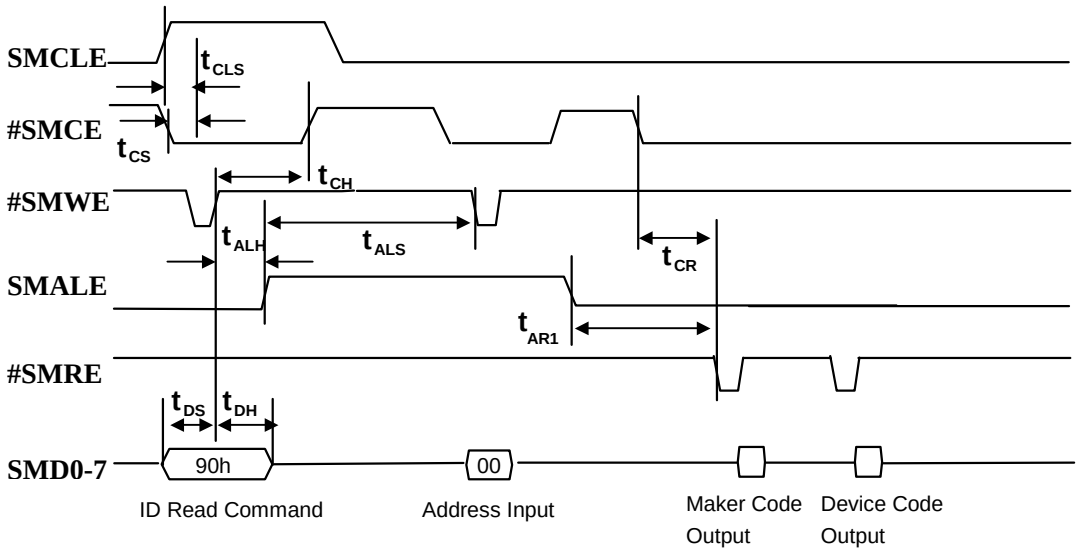
Read Cycle Timing

Read Cycle Timing in case #SMCE is set to High



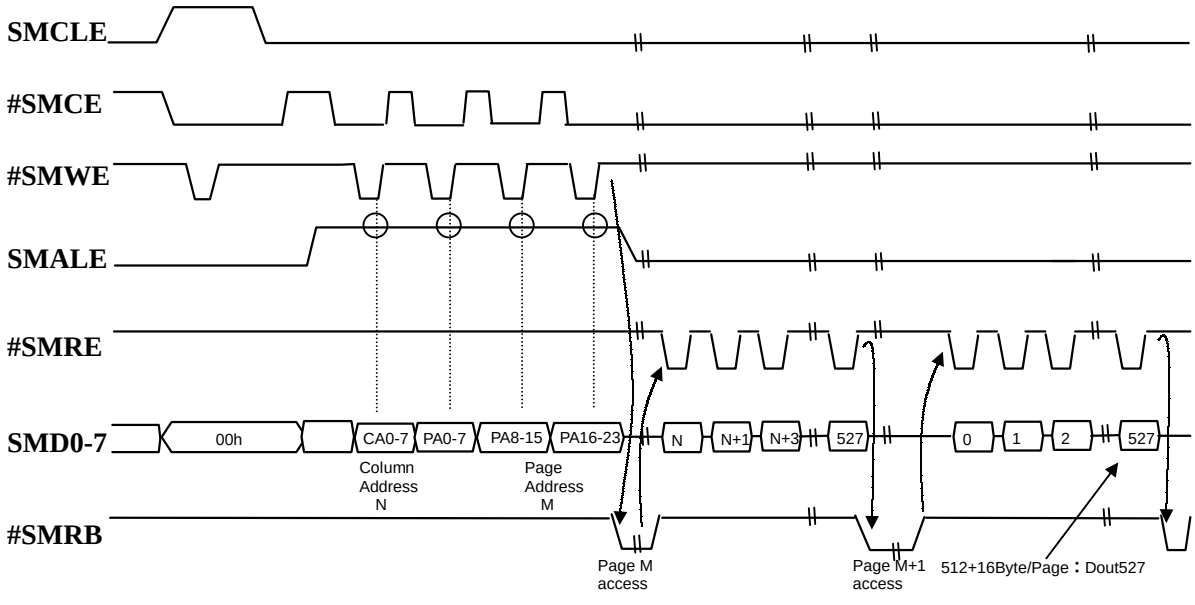
Read Cycle Timing in case #SMCE is set to High

ID Read Timing



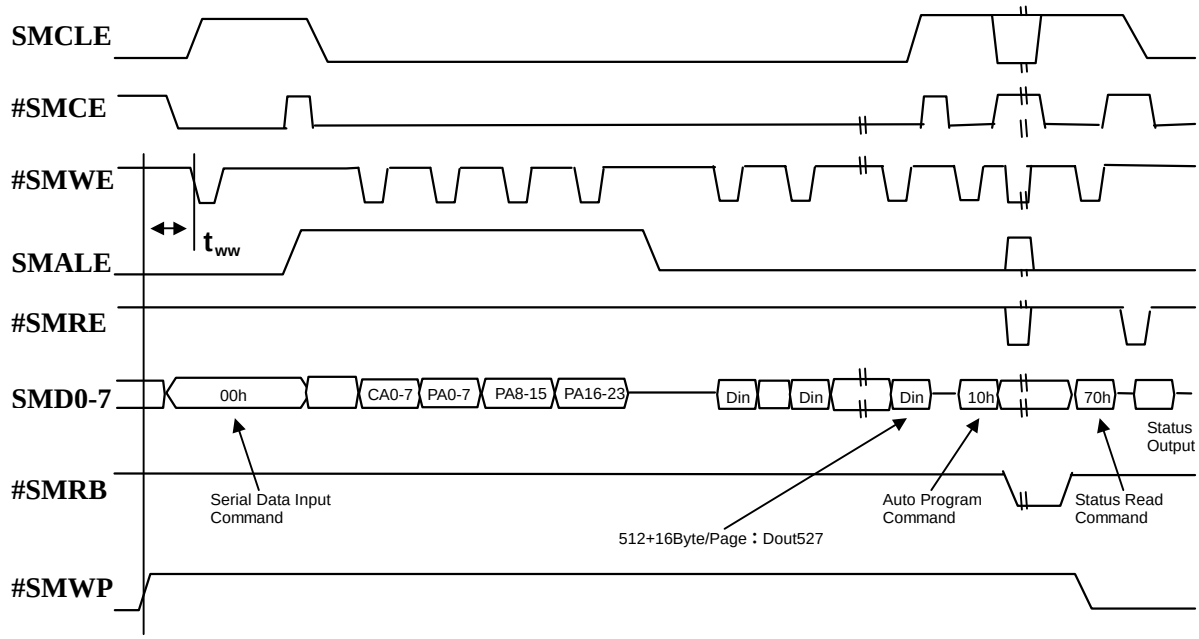
ID Read Timing

Sequential Read Timing



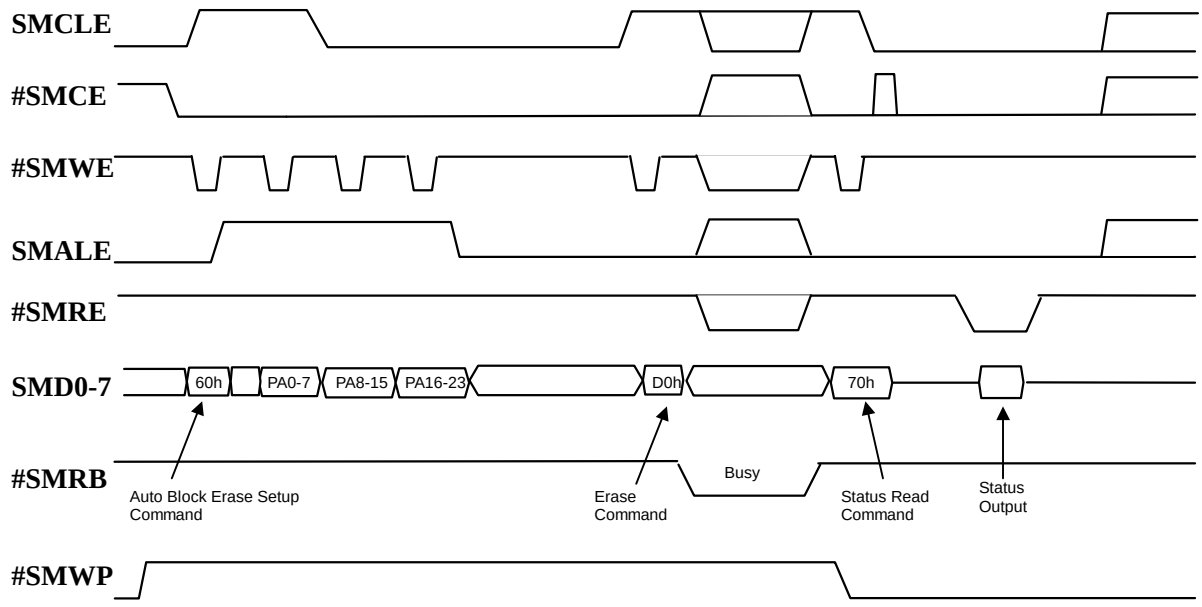
Sequential Read Timing

Auto Page Program Timing



Auto Page Program Timing

Auto Block Erase Timing



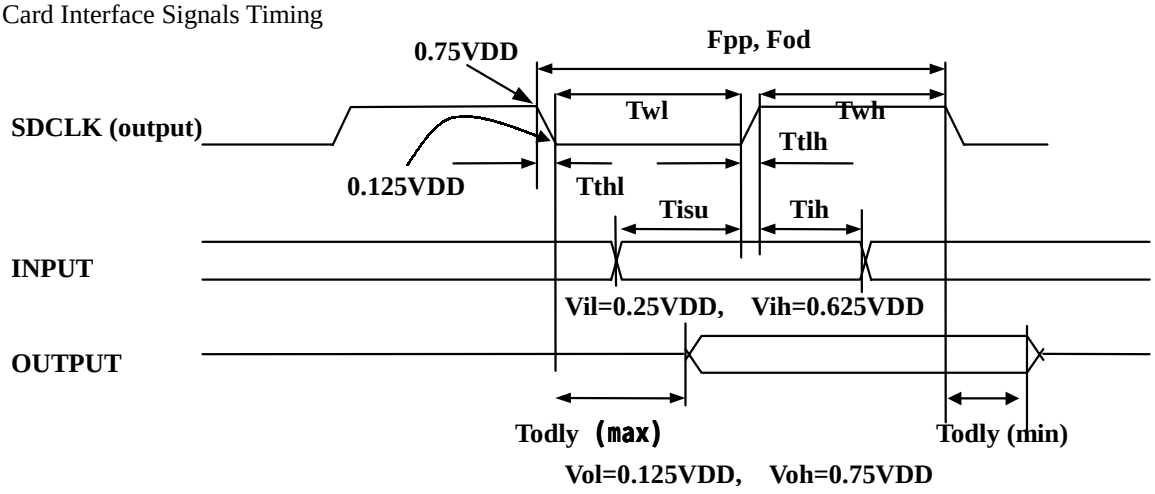
Auto Block Erase Timing

5.3.3 SD Card Interface Signal AC Characteristic

(VDD= V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Notes
	SDCD[3:0], SDCMD, SDCLK				
Fpp	Clock frequency Data Transfer Mode			MHz	Cl=
Fod	Clock frequency Identification Mode			KHz	Cl=
Twl	Clock Low time			ns	Cl=
Twh	Clock High time			ns	Cl=
Ttlh	Clock fall time			ns	Cl=
Tthl	Clock rise time			ns	Cl=
Tisu	Input set-up time			ns	Cl=
Tih	Input hold time			ns	Cl=
Todly	Output delay time			ns	Cl=

SD Card Interface Signals Timing



Timing for SD Card Interface Signals

5.3.4 USB Host Interface Signal AC Characteristic

(VDD= V, Ta= degree C)

T.B.D

5.3.5 Serial Port Interface Signal AC Characteristic

(VDD= V, Ta= degree C)

T.B.D

5.3.6 CompactFlash Control Interface Signal AC Characteristic

(VDD= V, Ta= degree C)

T.B.D

5.3.7 Low Polysilicon TFT-LCD Converter Interface Signal AC Characteristic
(VDD= V, Ta= degree C)

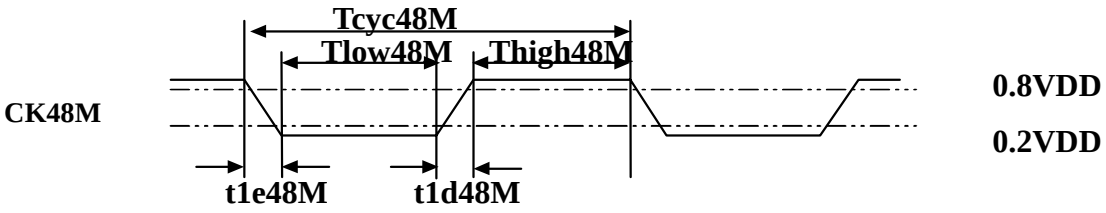
T.B.D

5.3.8 System Interface Signal AC Characteristic
(VDD= V, Ta= degree C)

CK48M AC Characteristic
(VDD= V, Ta= degree C)

Symbol	Parameter	Min	Max	Unit	Notes
	CK48M				
Tcyc48M	CLK cycle time			ns	
Thigh48M	CLK High time			ns	
Tlow48M	CLK Low time			ns	
t1d48M	CK48M Rising Time			ns	
t1e48M	CK48M Falling Time			ns	

CK48M Timing

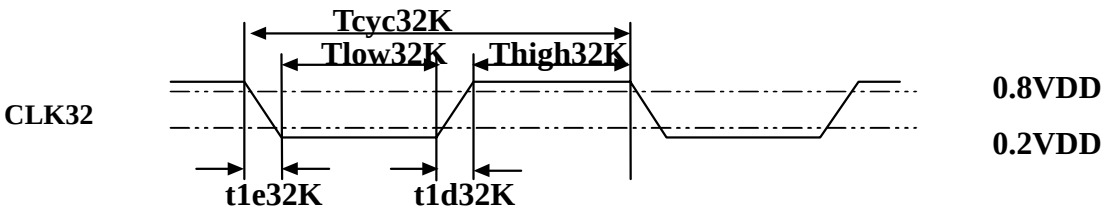


CLK32 AC Characteristic
(VDD= V, Ta= degree C)

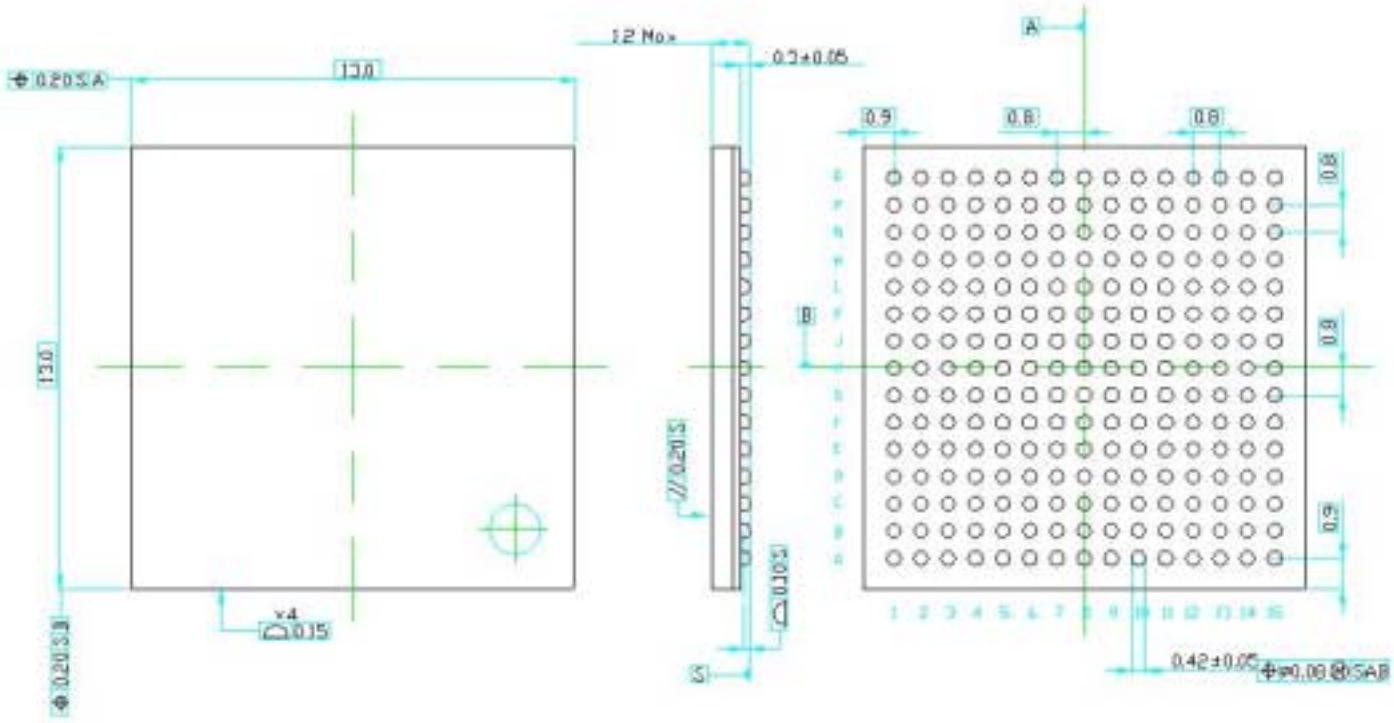
Symbol	Parameter	Min	Max	Unit	Notes
	CLK32				
Tcyc32K	CLK cycle time			us	
Thigh32K	CLK High time			us	
Tlow32K	CLK Low time			us	
t1d32K	CLK32 Rising Time			ns	
t1e32K	CLK32 Falling Time			ns	

T.B.D

CLK32 Timing



6. Package outline



Appendix

A. Reference diagram